

PRELIMINARY



ISD1700 Series

Multi-Message

Single-Chip

Voice Record & Playback Devices

Publication Release Date: February 7, 2006
Revision 1.2



TABLE OF CONTENTS

1	GENERAL DESCRIPTION	5
2	FEATURES.....	6
3	BLOCK DIAGRAM.....	7
4	PINOUT CONFIGURATION.....	8
5	PIN DESCRIPTION	9
6	FUNCTIONAL DESCRIPTION	13
6.1	Detailed Description.....	13
6.1.1	Audio Quality	13
6.1.2	Message Duration.....	13
6.1.3	Flash Storage	13
6.2	Memory Array Architecture	13
6.3	Modes of Operations.....	14
6.3.1	Standalone (Push-Button) Mode	14
6.3.2	SPI Mode	14
7	ANALOG PATH CONFIGURATION (APC).....	15
7.1	APC Register	15
7.2	Device Analog Path Configurations	16
8	STANDALONE (PUSH-BUTTON) OPERATIONS	17
8.1	Operation Overview	17
8.1.1	Record Operation	17
8.1.2	Playback Operation	18
8.1.3	Forward Operation.....	18
8.1.4	Erase Operation.....	19
8.1.5	Reset Operation.....	21
8.1.6	VOL Operation.....	21
8.1.7	FT (Feed-Through) Operation	21
8.2	vAlert Feature (Optional).....	21
8.3	Sound Effect (SE) Editing	21
8.3.1	Sound Effects (SEs)	21
8.3.2	Entering SE Mode.....	22
8.3.3	SE Editing	22
8.3.4	Exiting SE Mode	22
8.3.5	Sound Effect Duration.....	22
8.4	Analog Inputs	22

ISD1700 SERIES

8.4.1	Microphone Input.....	23
8.4.2	AnaIn Input.....	23
9	CIRCULAR MEMORY MANAGEMENT	24
9.1	Restoring Circular Memory Architecture.....	26
10	SERIAL PERIPHERAL INTERFACE (SPI) MODE	27
10.1	Microcontroller Interface	27
10.2	SPI Interface Overview	27
10.2.1	SPI Transaction Format.....	27
10.2.2	MOSI Data Format.....	28
10.2.3	MISO Data Format.....	29
10.3	SPI Command Overview.....	30
10.4	Switching from SPI mode to Standalone Mode	31
10.5	ISD1700 Device Registers.....	31
10.5.1	Status Register 0 (SR0).....	32
10.5.2	Status Register 1 (SR1).....	33
10.5.3	APC Register	33
10.5.4	Play Pointer.....	33
10.5.5	Record Pointer.....	34
10.5.6	DEVICEID Register	34
11	SPI COMMAND REFERENCE.....	35
11.1	SPI Priority Commands.....	36
11.1.1	PU Power Up (0x01).....	36
11.1.2	STOP (0x02).....	37
11.1.3	RESET (0x03).....	37
11.1.4	CLR_INT(0x04).....	37
11.1.5	RD_STATUS (0x05)	38
11.1.6	PD (0x07) Power Down	38
11.1.7	DEVID (0x09) Read Device ID	39
11.2	Circular Memory Commands	39
11.2.1	PLAY (0x40)	39
11.2.2	REC (0x41)	40
11.2.3	ERASE (0x42)	40
11.2.4	G_ERASE (0x43) Global Erase.....	40
11.2.5	FWD (0x48)	41
11.2.6	CHK_MEM (0x49) Check Circular Memory.....	41

ISD1700 SERIES

11.2.7	RD_PLAY_PTR (0x06)	42
11.2.8	RD_REC_PTR (0x08)	42
11.3	Analog Configuration Commands	42
11.3.1	RD_APC (0x44) Read APC Register	42
11.3.2	WR_APC1 (0x45) Load APC Register	43
11.3.3	WR_APC2 (0x65) Load APC Register	43
11.3.4	WR_NVCFG (0x46) Write APC to Non-Volatile Memory	44
11.3.5	LD_NVCFG (0x47) Load APC register from Non-Volatile Memory	44
11.4	Direct Memory Access Commands	44
11.4.1	SET_PLAY (0x80)	45
11.4.2	SET_REC (0x81)	45
11.4.3	SET_ERASE (0x82)	46
11.5	Additional Command	46
12	TIMING DIAGRAMS	47
12.1	Record, play and erase	47
13	ABSOLUTE MAXIMUM RATINGS	51
13.1	Operating Conditions	52
14	ELECTRICAL CHARACTERISTICS	53
14.1	DC Parameters	53
14.2	AC Parameters	54
15	TYPICAL APPLICATION CIRCUITS	55
15.1	Good Audio Design Practices	58
16	PACKAGING	59
16.1	28-Lead 8x13.4mm Plastic Thin Small Outline Package (TSOP) Type 1 - IQC	59
16.2	28-Lead 300-Mil Plastic Small Outline Integrated Circuit (SOIC)	60
16.3	28-Lead 600-Mil Plastic Dual Inline Package (PDIP)	61
16.4	Die Information	61
17	ORDERING INFORMATION	62
18	VERSION HISTORY	63

ISD1700 SERIES



1 GENERAL DESCRIPTION

The Winbond® ISD1700 ChipCorder® Series is a high quality, fully integrated, single-chip multi-message voice record and playback device ideally suited to a variety of electronic systems. The message duration is user selectable in ranges from 26 seconds to 120 seconds, depending on the specific device. The sampling frequency of each device can also be adjusted from 4 kHz to 12 kHz with an external resistor, giving the user greater flexibility in duration versus recording quality for each application. Operating voltage spans a range from 2.4 V to 5.5 V to ensure that the ISD1700 devices are optimized for a wide range of battery or line-powered applications.

The ISD1700 is designed for operation in either standalone or microcontroller (SPI) mode. The device incorporates a proprietary message management system that allows the chip to self-manage address locations for multiple messages. This unique feature provides sophisticated messaging flexibility in a simple push-button environment. The devices include an on-chip oscillator (with external resistor control), microphone preamplifier with Automatic Gain Control (AGC), an auxiliary analog input, anti-aliasing filter, Multi-Level Storage (MLS) array, smoothing filter, volume control, Pulse Width Modulation (PWM) Class D speaker driver, and current output.

The ISD1700 devices also support an optional "vAlert" (voiceAlert) feature that can be used as a new message indicator. With vAlert, the IC strobes an external LED to indicate that a new message is present. Four special sound effect locations are reserved for audio confirmation of commands, such as "Start Record", "Stop Record," and "Erase."

Recordings are stored in on-chip Flash memory cells, providing zero-power message storage. This unique single-chip solution is made possible through Winbond's patented Multi-Level Storage (MLS) technology. Audio data are stored directly in solid-state memory without digital compression, providing superior quality voice and music reproduction.

Voice signals can be fed into the chip through two independent paths: a differential microphone input and a single-ended analog input. For outputs, the ISD1700 provides a Pulse Width Modulation (PWM) Class D speaker driver and a separate analog output simultaneously. The PWM can directly drive a standard 8Ω speaker or typical buzzer, while the separate analog output can be configured as a single-ended current or voltage output to drive an external amplifier.

The ISD1700 devices automatically enter into power down mode for power conservation when an operation is completed.

In the SPI mode, the user has full control via the serial interface in operating the device. This includes random access to any location inside the memory array by specifying the start address and end address of operations. SPI mode also allows access to the Analog Path Configuration (APC) register. This register allows flexible configuration of audio paths, inputs, outputs and mixing. The APC default configuration for standalone mode can also be modified by storing the APC to a non-volatile register (NVCFG) that is loaded at initialization. Utilizing the capabilities of ISD1700 Series, designers have the control and flexibility to implement high-end products.

Notice: The specifications are subject to change without notice. Please contact Winbond Sales Offices or Representatives to verify current or future specifications. Also refer to the website for any related application notes.



2 FEATURES

- Integrated message management systems for single-chip, push-button applications
 - $\overline{\text{REC}}$: level-trigger for recording
 - $\overline{\text{PLAY}}$: edge-trigger for individual message or level-trigger for sequential playback
 - $\overline{\text{ERASE}}$: edge-triggered erase for first or last message or level-triggered erase for all messages
 - $\overline{\text{FWD}}$: edge-trigger to advance to the next message or fast message scan during the playback
 - $\overline{\text{VOL}}$: 8 levels output volume control
 - $\text{RDY}/\overline{\text{INT}}$: ready or busy status indication
 - $\overline{\text{RESET}}$: bring back to the default state
 - Automatic power-down after each operation cycle

- Selectable sampling frequency controlled by an external oscillator resistor

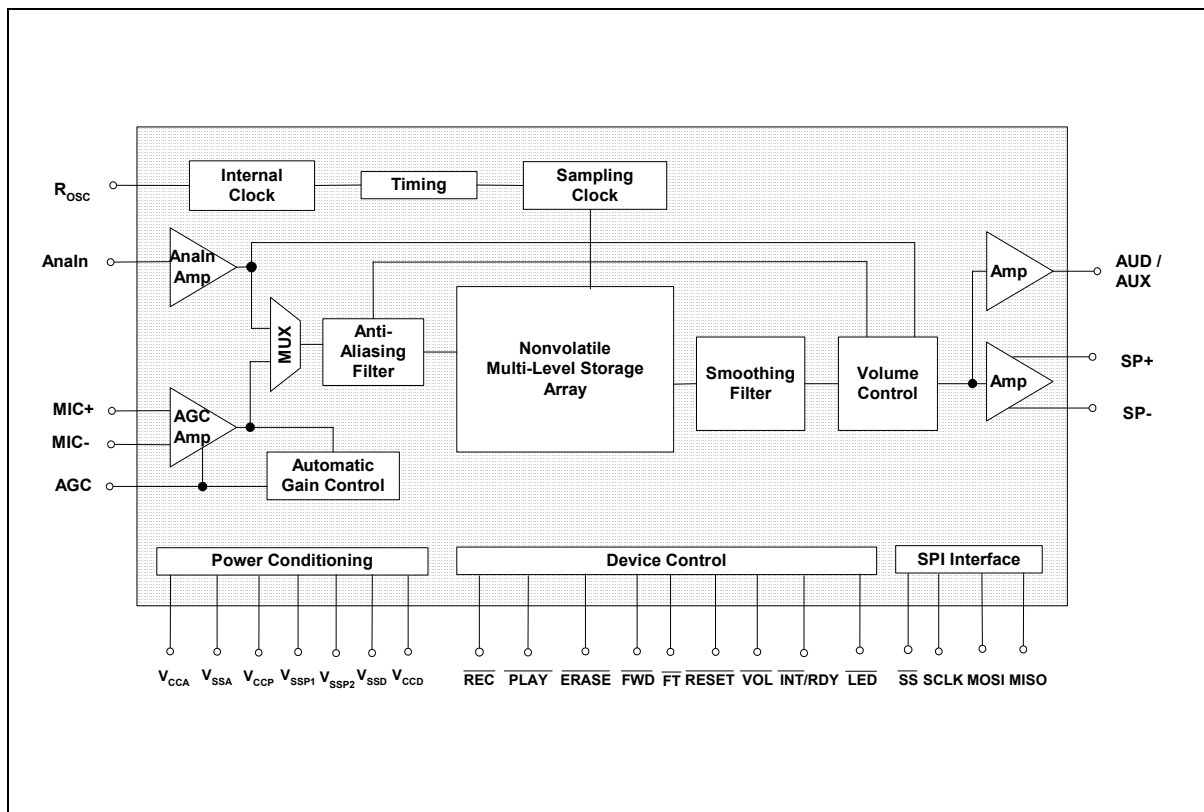
Sampling Frequency	12 kHz	8 kHz	6.4 kHz	5.3 kHz	4 kHz
Rosc	60 k Ω	80 k Ω	100 k Ω	120 k Ω	160 k Ω

- Selectable message duration
 - A wide range selection from 30 secs to 240 secs at 8 kHz sampling frequency
- Message and operation indicators
 - Four customizable Sound Effects (SE) for audible indications
 - Optional vAlert (voiceAlert) to indicate the presence of new messages
 - LED: stay on during recording, blink during playback, forward and erase operations
- Dual operating modes
 - *Standalone mode*:
 - Integrated message management techniques
 - Automatic power-down after each operation cycle
 - *SPI mode*:
 - Fully user selectable and controllable options via Analog Path Configuration (APC) register
- Two individual input channels
 - MIC+/MIC-: differential microphone inputs with AGC (Automatic Gain Control)
 - Analn: single-ended auxiliary analog input for recording or feed-through
- Dual output channels
 - PWM Class D speaker amplifier to directly drive an 8 Ω speaker or a typical buzzer
 - Configurable AUD (current) or AUX (voltage) single-ended output drive external power amplifier
- ChipCorder standard features
 - High-quality, natural voice and audio reproduction
 - 2.4V to 5.5V operating voltage
 - 100-year message retention (typical)
 - 100,000 record cycles (typical)
- Temperature options:
 - Commercial: 0°C to +50°C (die); 0°C to +70°C (packaged units)
 - Industrial: -40°C to +85°C (packaged units)
- Package options: Lead-free packaged units
- Package types: available in die, PDIP, SOIC and TSOP

ISD1700 SERIES



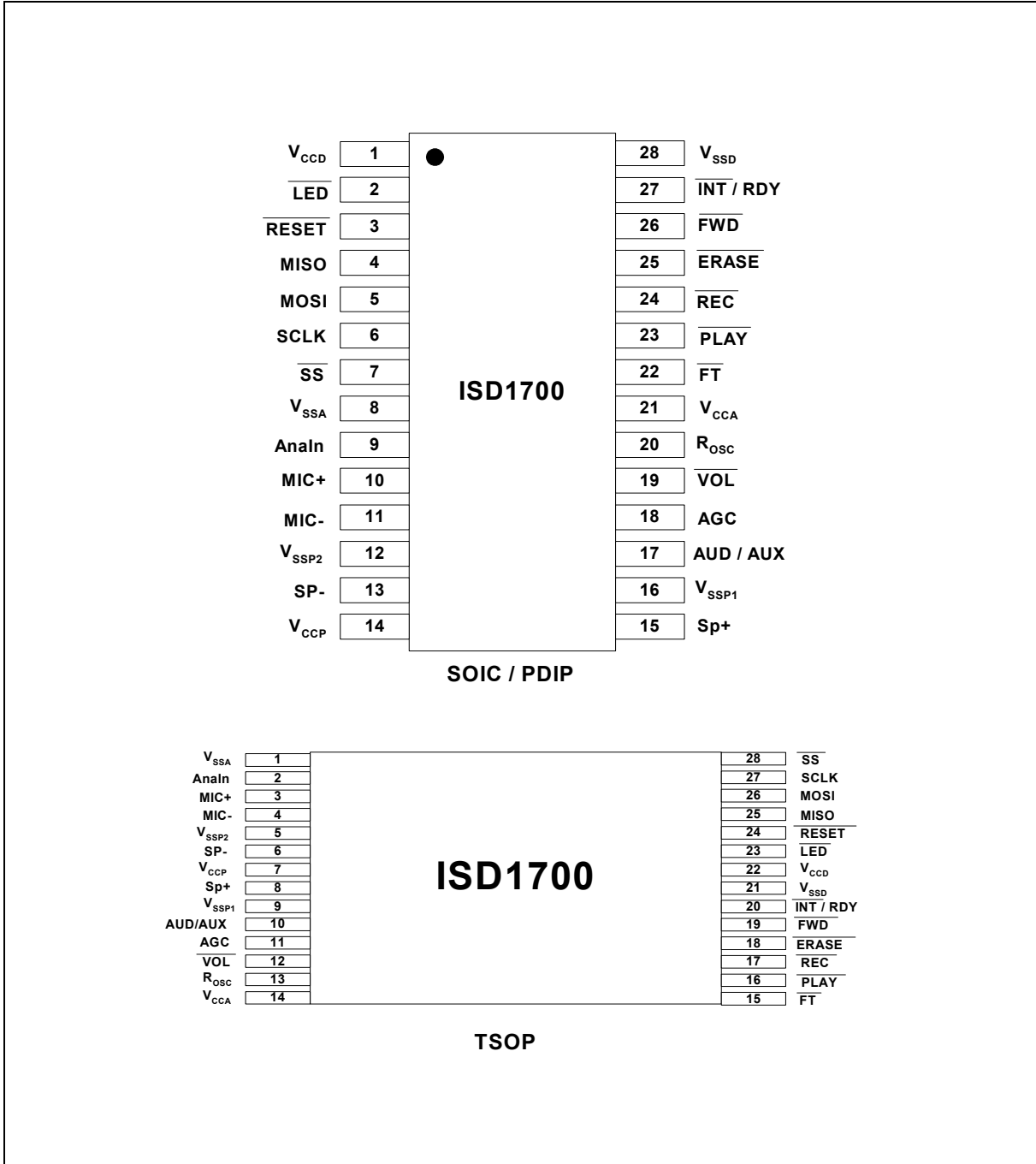
3 BLOCK DIAGRAM



ISD1700 SERIES



4 PINOUT CONFIGURATION



ISD1700 SERIES



5 PIN DESCRIPTION

PIN NAME	PDIP / SOIC	TSOP	FUNCTIONS
V _{CCD}	1	22	Digital Power Supply: It is important to have a separate path for each power signal including V _{CCD} , V _{CCA} and V _{CCP} to minimize the noise coupling. Decoupling capacitors should be as close to the device as possible.
$\overline{\text{LED}}$	2	23	LED: This output turns on an LED during a record cycle and blinks LED during playback, forward and erase operations.
$\overline{\text{RESET}}$	3	24	RESET: When Low, the device enters into a known state and initializes all pointers to the default state. This pin has an internal pull-up resistor ^[1] .
MISO	4	25	Master In Slave Out: The I1700 places data on the MISO line one half-cycle before the falling edge of SCLK. Data is shifted out on the falling edge of SCLK. When the SPI is inactive ($\overline{\text{SS}} = \text{high}$), it's tri-state.
MOSI	5	26	Master Out Slave In: Data input of the SPI interface when the device is configured as slave. The master microcontroller places data on the MOSI line one half-cycle before the rising edge of SCLK. Data is latched into the device on the rising edge of SCLK. When not used, it should be tied High.
SCLK	6	27	Serial Clock: Clock of the SPI interface. It is usually generated by the master device (typically microcontroller) and is used to synchronize the data transfer in and out of the device through the MOSI and MISO lines, respectively. When not used, it should be tied High.
$\overline{\text{SS}}$	7	28	Slave Select: This input, when low, selects the device as slave device and enables the SPI interface. When not used, it should be tied High.
V _{SSA}	8	1	Analog Ground: It is important to have a separate path for each ground signal including V _{SSA} , V _{SSD} , V _{SSP1} and V _{SSP2} to minimize the noise coupling.
Analn	9	2	Analn: Auxiliary analog input to the device for recording or feed-through. An AC-coupling capacitor (typical 0.1uF) is necessary and the amplitude of the input signal should not exceed 1.0 V _{pp} . Depending upon the D3 of APC register, Analn signal can be directly recorded into the memory, mixed with the Mic signal then recorded into the memory or buffered to the speaker and AUD/AUX outputs via feed-through path.
MIC+	10	3	MIC+: Non-inverting input of the differential microphone signal. The input signal should be AC-coupled to this pin via a series capacitor. The capacitor value, together with an internal 10 K Ω resistance on this pin, determines the low-frequency cutoff for the pass band filter. The Mic analog path is also controlled by D4 of APC register.
MIC-	11	4	MIC-: Inverting input of the differential microphone signal. The input signal should be AC-coupled to the MIC+ pin. It provides input noise-cancellation, or common-mode rejection, when the microphone is connected differentially to the device. The Mic analog path is also controlled by D4 of APC register.

ISD1700 SERIES



PIN NAME	PDIP / SOIC	TSOP	FUNCTIONS
V _{SSP2}	12	5	Ground for Negative PWM Speaker Driver: It is important to have a separate path for each ground signal including V _{SSA} , V _{SSD} , V _{SSP1} and V _{SSP2} to minimize the noise coupling.
SP-	13	6	SP-: The negative Class D PWM provides a differential output with SP+ pin to directly drive an 8 Ω speaker or typical buzzer. During power down or recording, this pin is tri-stated. This output can be controlled by D8 of APC register. The factory default is set at on state.
V _{CCP}	14	7	Power Supply for PWM Speaker Driver: It is important to have a separate path for each power signal including V _{CCD} , V _{CCA} and V _{CCP} to minimize the noise coupling. Decoupling capacitors to V _{SSP1} and V _{SSP2} should be as close to the device as possible. The V _{CCP} supply and V _{SSP} ground pins have large transient currents and need low impedance returns to the system supply and ground, respectively.
SP+	15	8	SP+: The positive Class D PWM provides a differential output with the SP- pin to directly drive an 8 Ω speaker or typical buzzer. During power down or recording, this pin is tri-stated. This output can be controlled by D8 of APC register. The factory default is set at on state.
V _{SSP1}	16	9	Ground for Positive PWM Speaker Driver: It is important to have a separate path for each ground signal including V _{SSA} , V _{SSD} , V _{SSP1} and V _{SSP2} to minimize the noise coupling.
AUD/ AUX	17	10	Auxiliary Output: Depending upon the D7 of APC register, this output is either an AUD or AUX output. AUD is a single-ended current output, whereas AUX is a single-ended voltage output. They can be used to drive an external amplifier. The factory default is set at AUD. This output can be powered down by D9 of APC register. The factory default is set at on state.
AGC	18	11	Automatic Gain Control (AGC): The AGC adjusts the gain of the preamplifier dynamically to compensate for the wide range of microphone input levels. The AGC allows the full range of signals to be recorded with minimal distortion. The AGC is designed to operate with a nominal capacitor of 4.7 μF connected to this pin. Connecting this pin to ground (V _{SSA}) provides maximum gain to the preamplifier circuitry. Conversely, connecting this pin to the power supply (V _{CCA}) provides minimum gain to the preamplifier circuitry.
$\overline{\text{VOL}}$	19	12	Volume: This control has 8 steps of volume adjustment. Each Low going pulse decreases the volume by one level. Repeated pulses decrease volume level from current setting to minimum then increase back to maximum, and continue this loop. During power-up or $\overline{\text{RESET}}$, a default setting is loaded from non-volatile configuration. The factory default is set at maximum. This output can also be controlled by <D2:D0> of APC register. This pin has an internal pull-up device ^[1] . This input has internal debounce (T _{Deb}) ^[2] for start and end allowing the use of a push button switch.

ISD1700 SERIES



PIN NAME	PDIP / SOIC	TSOP	FUNCTIONS
R _{OSC}	20	13	Oscillator Resistor: A resistor connected from R _{OSC} pin to ground determines the sample frequency of the device, which sets the duration. Please refer to the Duration Section for details.
V _{CCA}	21	14	Analog Power Supply. It is important to have a separate path for each power signal including V _{CCD} , V _{CCA} and V _{CCP} to minimize the noise coupling. Decoupling capacitors to V _{SSA} should be as close to the device as possible.
$\overline{\text{FT}}$	22	15	Feed-through: In Standalone mode, when FT is engaged low, the AnIn feed-through path is activated. As a result, the AnIn signal is transmitted directly from AnIn to both Speaker and AUD/AUX outputs with Volume Control. However, SPI overrides this input, while in SPI mode, and feed-through path is controlled by a D6 of APC register. This pin has an internal pull-up device ^[1] and an internal debounce (T _{Deb}) ^[2] for start and end allowing the use of a push button switch.
$\overline{\text{PLAY}}$	23	16	Playback: Pulsing $\overline{\text{PLAY}}$ to Low once initiates a playback operation. Playback stops automatically when it reaches the end of the message. Pulsing it to Low again during playback stops the operation. Holding $\overline{\text{PLAY}}$ Low constantly functions as a sequential playback operation loop. This looping continues until $\overline{\text{PLAY}}$ returns to High. This pin has an internal pull-up device ^[1] and an internal debounce (T _{Deb}) ^[2] for start and end, allowing the use of a push button switch.
$\overline{\text{REC}}$	24	17	Record: The device starts recording whenever $\overline{\text{REC}}$ switches from High to Low and stays at Low. Recording stops when the signal returns to High. This pin has an internal pull-up device ^[1] and an internal debounce (T _{Deb}) ^[2] for start and end, allowing the use of a push button switch.
$\overline{\text{ERASE}}$	25	18	Erase: When active, it starts an erase operation. Erase operation will take place only when the playback pointer is positioned at either the first or last message. Pulsing this pin to Low enables erase operation and deletes the current message. Holding this pin Low for more than 3 sec. initiates a global erase operation, and will delete all the messages. This pin has an internal pull-up device ^[1] and an internal debounce (T _{Deb}) ^[2] for start and end, allowing the use of a push button switch.
$\overline{\text{FWD}}$	26	19	Forward: When triggered, it advances to the next message from the current location, when the device is in power down status. During playback cycle, pulsing this pin Low stops the current playback operation and advances to the next message, and then re-starts the playback operation of the new message. This pin has an internal pull-up device ^[1] and an internal debounce (T _{Deb}) ^[2] for start and end, allowing the use of a push button switch.

ISD1700 SERIES



PIN NAME	PDIP / SOIC	TSOP	FUNCTIONS
RDY/ $\overline{\text{INT}}$	27	20	<p>An open drain output.</p> <p>Ready (Standalone mode): This pin stays Low during record, play, erase and forward operations and stays High in power down state</p> <p>Interrupt (SPI mode): After completing the SPI command, an active low interrupt is generated. Once the interrupt is cleared, it returns to High.</p>
V _{SSD}	28	21	<p>Digital Ground: It is important to have a separate path for each ground signal including V_{SSA}, V_{SSD}, V_{SPP1} and V_{SPP2} to minimize the noise coupling.</p>

Note: ^[1] 600 k Ω

^[2] TDeb = Refer to AC Timing

ISD1700 SERIES



6 FUNCTIONAL DESCRIPTION

6.1 DETAILED DESCRIPTION

6.1.1 Audio Quality

Winbond's patented ChipCorder[®] Multi-Level Storage (MLS) technology provides a natural, high-quality record and playback solution on a single chip. The input voice signals are stored directly in the Flash memory and are reproduced in their natural form without any of the compression artifacts caused by digital speech solutions.

6.1.2 Message Duration

The ISD1700 Series offer record and playback duration from 26 seconds to 120 seconds. Sampling rate and message duration are determined by an external resistor connected to the R_{osc} pin.

Table 6.1 Duration vs. Sampling Frequency

Sample Rate	ISD1730	ISD1740	ISD1750	ISD1760	ISD1790	ISD17120	ISD17150	ISD17180	ISD17210	ISD17240
12 kHz	20 secs	26 secs	33 secs	40 secs	60 secs	80 secs	100 secs	120 secs	140 secs	160 secs
8 kHz	30 secs	40 secs	50 secs	60 secs	90 secs	120 secs	150 secs	180 secs	210 secs	240 secs
6.4 kHz	37 secs	50 secs	62 secs	75 secs	112 secs	150 secs	187 secs	225 secs	262 secs	300 secs
5.3 kHz	45 secs	60 secs	75 secs	90 secs	135 secs	181 secs	226 secs	271 secs	317 secs	362 secs
4 kHz	60 secs	80 secs	100 secs	120 secs	180 secs	240 secs	300 secs	360 secs	420 secs	480 secs

6.1.3 Flash Storage

The ISD1700 devices utilize embedded Flash memory to provide non-volatile storage. A message can be retained for a minimum of 100 years without power. Additionally, each device can be re-recorded over 100,000 times (typical).

6.2 MEMORY ARRAY ARCHITECTURE

The memory array provides storage of four special Sound Effects (SE) as well as the voice data. The memory array is addressed by rows. A row is the minimum storage resolution by which the memory can be addressed. The memory assignment is automatically handled by the internal message management system in standalone mode. While in SPI mode, one has the full access to the entire memory via the eleven address bits. The minimum storage resolution varies with the sampling frequency, as shown in Table 6.2.

Table 6.2 Minimum Storage Resolution vs. Sampling Frequency

Sampling Frequency	12 kHz	8 kHz	6.4 kHz	5.3 kHz	4 kHz
Minimum Storage Resolution	83.3 msec	125 msec	156 msec	187 msec	250 msec

For example, at 8 kHz sampling frequency, the minimum storage resolution is 125 msec, so each Sound Effect (SE) is approximately 0.5 second long.

The four sound effects occupy the first sixteen rows in the memory array with four rows for each SE. That means from address 0x000 to address 0x00F. The remaining memory is dedicated to

ISD1700 SERIES



voice data storage. Hence, the voice message storage address will be from 0x010 to the end of memory array. Table 6.3 shows the maximum row address for each device in the ISD1700 family.

Table 6.3 Device Maximum Row Address

Device	ISD1730	ISD1740	ISD1750	ISD1760	ISD1790	ISD17120	ISD17150	ISD17180	ISD17210	ISD17240
Maximum Address	0x0FF	0x14F	0x19F	0x1EF	0x2DF	0x3CF	0x4BF	0x5AF	0x69F	0x78F

Due to the nature of the voice message applications, the memory array may be able to tolerate a certain number of non-programmable memory cells existed randomly. The allowable number of non-programmable cells for each device are as follows: four for ISD1730, four for ISD1740, four for ISD1750, four for ISD1760, eight for ISD1790, eight for ISD17120, eight for ISD17150, ten for ISD17180, ten for ISD17210 and ten for ISD17240.

6.3 MODES OF OPERATIONS

The ISD1700 Series can operate in either Standalone (Push-Button) or microcontroller (SPI) mode.

6.3.1 Standalone (Push-Button) Mode

Standalone operation entails use of the $\overline{\text{REC}}$, $\overline{\text{PLAY}}$, $\overline{\text{FT}}$, $\overline{\text{FWD}}$, $\overline{\text{ERASE}}$, $\overline{\text{VOL}}$ and $\overline{\text{RESET}}$ pins to trigger operations. The internal state machine automatically configures the audio path according to the desired operation. In this mode, the internal state machine takes full control on message management. This allows the user to record, playback, erase, and forward messages without the needs to know the exact addresses of the messages stored inside the memory. For additional information, please refer to Section 8.

6.3.2 SPI Mode

In SPI mode, control of the device is achieved through the 4-wire serial interface. Commands similar to the push button controls, such as $\overline{\text{REC}}$, $\overline{\text{PLAY}}$, $\overline{\text{FT}}$, $\overline{\text{FWD}}$, $\overline{\text{ERASE}}$, $\overline{\text{VOL}}$ and $\overline{\text{RESET}}$, can be executed through the SPI interface. In addition, there are commands that allow the modification of the analog path configuration and commands that direct access the memory address of the array, plus others. The SPI mode allows more control over the operations of the device and the ability to perform complex message management rather than conform to the circular memory constraints of push-button mode. Refer to SPI sections for details.

ISD1700 SERIES



7 ANALOG PATH CONFIGURATION (APC)

The analog path of the ISD1700 can be configured to accommodate a wide variety of signal path possibilities. This includes the source of recording signals, mixing of input signals, mixing the playback signal with an input signal to the outputs, feed-through signal to the outputs and which outputs being activated.

The active analog path configuration is determined by a combination of the internal state of the device, i.e. desired operation (record or playback), the status of the \overline{FT} and the contents of the APC register. The APC register is initialized by the internal non-volatile configuration (NVCFG) bits upon power-on-reset or reset function. The APC register can be read and loaded using SPI commands.

The factory default of NVCFG bits, <D11:D0>, is 0100 0100 0000 = 0x440. This configures the device with recording through the MIC inputs, FT via Analn input, playback from MLS, SE editing feature enabled, maximum volume level, active PWM driver and AUD current outputs. One can use SPI commands to modify the APC register and store it permanently into the NVCFG bits.

7.1 APC REGISTER

Details of the APC register are shown in Table 7.1.

Table 7.1 APC Register

Bit	Name	Description	Default
D0	VOL0	Volume control bits <D2:D0>: These provide 8 steps of -4dB per step volume adjustment. Each bit changes the volume by one step, where 000 = maximum and 111 = minimum.	000 (maximum)
D1	VOL1		
D2	VOL2		
D3	Monitor_Input	Monitor input signal at outputs during recording.	0 = Monitor_input is Disabled
		D3 = 0 \overline{FT} / D6= 0 Analn REC	
		D3 = 1 \overline{FT} / D6= 1 Mic REC	
D4	Mix_Input	Combined with \overline{FT} in standalone mode or SPI_FT bit (D6) in SPI mode, D4 controls the input selection for recording.	0 = Mix_Input is Off
		D4 = 0 \overline{FT} / D6= 0 Analn REC	
		\overline{FT} / D6= 1 Mic REC	
		D4 = 1 \overline{FT} / D6= 0 (Mic + Analn) REC	
	\overline{FT} / D6= 1 Mic REC		
D5	SE_Editing	Enable or disable editing of Sound Effect in Standalone mode: where 0 = Enable, 1 = Disable	0 = Enable SE_Editing

ISD1700 SERIES



Bit	Name	Description	Default	
D6	SPI_FT	For SPI mode only. Once SPI_PU command is sent, the \overline{FT} is disabled and replaced by this control bit (D6) with the same functionality. After exiting SPI mode through the PD command, the \overline{FT} resumes control of feedthrough (FT) function.	1 = SPI FT is Off	
		D6 = 0		FT function in SPI mode is On
		D6 = 1		FT function in SPI mode is Off
D7	Analog Output: AUD/AUX	Select AUD or AUX: 0 = AUD, 1 = AUX	0 = AUD	
D8	PWM SPK	PWM Speaker +/- outputs: 0 = Enabled, 1 = Disabled	0 = PWM enabled	
D9	PU Analog Output	PowerUp analog output: 0 = On, 1 = Off	0 = On	
D10	vAlert	vAlert: 0 = On, 1 = Off.	1 = Off	
D11	EOM Enable	EOM Enable for SetPlay operation: 0 = Off, 1 = On. When this bit is set to 1, SetPlay operation will stop at EOM location, rather than the End Address.	0 = Off	

7.2 DEVICE ANALOG PATH CONFIGURATIONS

Table 7.2 demonstrates the possible analog path configurations with ISD1700. The device can be in power-down, power-up, recording, playback and/or feed-through state depending upon the operation requested by the push-buttons or related SPI commands. The active path in each of these states is determined by D3 and D4 of the APC register, as well as either D6 of the APC register in SPI mode or the \overline{FT} status in standalone mode. In addition, D7~D9 of the APC register determine which output drivers are activated.

Table 7.2 Operational Paths

APC Register			Operational Paths		
D6/ \overline{FT}	D4 Mix	D3 Mon	Idle	Record	Playback
0	0	0	Analn FT	Analn Rec	(Analn + MLS) --> o/p
0	0	1	Analn FT	Analn Rec + Analn FT	(Analn + MLS) --> o/p
0	1	0	(Mic + Analn) FT	(Mic + Analn) Rec	(Analn + MLS) --> o/p
0	1	1	(Mic + Analn) FT	(Mic + Analn) Rec + (Mic + Analn) FT	(Analn + MLS) --> o/p
1	0	0	FT Disable	Mic Rec	MLS --> o/p
1	0	1	FT disable	Mic Rec + Mic FT	MLS --> o/p
1	1	0	FT disable	Mic Rec	MLS --> o/p
1	1	1	FT disable	Mic Rec + Mic FT	MLS --> o/p

ISD1700 SERIES



8 STANDALONE (PUSH-BUTTON) OPERATIONS

The user utilizes the $\overline{\text{REC}}$, $\overline{\text{PLAY}}$, $\overline{\text{FT}}$, $\overline{\text{FWD}}$, $\overline{\text{ERASE}}$, $\overline{\text{VOL}}$ or $\overline{\text{RESET}}$ pin to initiate an operation. The device automatically enters the power-down state at the end of a PLAY, REC, ERASE, FWD, VOL, or RESET operation.

8.1 OPERATION OVERVIEW

After power-on-reset (POR), the device is in the factory default state and two internal record and playback pointers are initialized. (Detailed information about these two pointers is provided later in this Section.) Then, the active analog path configuration is determined by the state of the $\overline{\text{FT}}$, and by the status of the APC register.

Up to four optional sound effects (SE1-4) can be programmed into the device to provide audible feedback to alert the user about the operating status. Separately, the LED output provides visual feedback on the operating state even if no sound effects are programmed. During the active state of LED output, no new commands will be accepted.

A circular message management technique is implemented. Recorded messages are stored sequentially into the memory from the beginning to the end in a circular manner.

Two internal pointers, the record pointer and playback pointer, determine the point at which an operation starts. After POR or $\overline{\text{RESET}}$, these pointers are initialized as follows:

- If no messages are present, both point to the beginning.
- If messages are present, the record pointer points to the next available memory location after the last message and the playback pointer points to the beginning of the last recorded message.

The playback pointer is affected primarily by the $\overline{\text{FWD}}$ operation. The record pointer is updated to the next available memory location after each $\overline{\text{REC}}$ operation.

8.1.1 Record Operation

Recording is controlled by the $\overline{\text{REC}}$. Setting this pin Low starts a record operation. The device will start recording from the next available location in memory and will continue recording until either the $\overline{\text{REC}}$ is returned High or the memory becomes full. The source of the recording is from either MIC or AnIn, whereas the active analog configuration path is determined by the desired operation and the state of the $\overline{\text{FT}}$. The $\overline{\text{REC}}$ is debounced internally. After recording, the record pointer will move from the last recorded message to the next available address and the playback pointer will be positioned at the beginning of the newly recorded message.

It is important for an Erase operation to be performed on the desired location before any recording proceeds. Also, the power supply must remain On during the entire process of recording. If power is interrupted during recording, the LED will blink seven times, which indicates that something unusual has occurred. In this event, performing a Global Erase will reset the chip back to its proper state.

Message record indicators:



- a) When $\overline{\text{REC}}$ goes Low:
 - If present, SE1 is played and LED flashes once.
 - Then, the LED stays On to indicate that a recording is in progress.
- b) When $\overline{\text{REC}}$ goes High or when the memory is full:
 - If present, SE2 is played and the LED flashes twice, and then remains Off to alert the user that the recording process has been completed.

Triggering of $\overline{\text{REC}}$ during a play, erase or forward operation is an illegal operation and will be ignored.

8.1.2 Playback Operation

Two playback modes are executed by $\overline{\text{PLAY}}$, which is internally debounced.

- a) **Edge-trigger mode:** Pulsing $\overline{\text{PLAY}}$ Low once initiates a playback operation of the current message. Playback automatically stops at the end of the message. Pulsing $\overline{\text{PLAY}}$ again will re-play the message. During playback, the LED flashes and goes Off when the operation stops. Pulsing $\overline{\text{PLAY}}$ to Low again during playback stops the operation. Under these circumstances, the playback pointer remains at the start of the played message after the operation is completed.
- b) **Sequential Playback mode:** If $\overline{\text{PLAY}}$ is held Low constantly, all messages will be played and looped from the current message to its previous message. This looping continues until $\overline{\text{PLAY}}$ is released. After each message, SE1 is played. After the last message has been played, SE2 is played, and then device plays the first message again. During the entire playback operation, the LED flashes. When playback stops, the playback pointer will be placed at the start of the halted message.

Triggering $\overline{\text{PLAY}}$ during a record, erase, or forward operation is an illegal operation and will be ignored.

8.1.3 Forward Operation

The $\overline{\text{FWD}}$ allows the user to move the playback pointer to the next message in a forward direction. When the pointer reaches the last message, it will jump back to the first message. Hence, the movement is in a circular fashion among the messages. The $\overline{\text{FWD}}$ is debounced internally. The effect of a Low-going pulse on the $\overline{\text{FWD}}$ depends on the current state of the device:

- a) If the device is in power-down state and the current location of the playback pointer is *not* the last message: the pointer will advance one message and, if present, SE1 is played. The LED flashes once.
- b) If the device is in power-down state and the current location of the play pointer is the last message: the pointer will advance to the first message and, if present, SE2 is played. The LED will flash twice.
- c) If the device is currently playing a message that is not the last one:
 - Playback is halted.

ISD1700 SERIES



- The playback pointer is advanced one message.
 - If present, SE1 is played.
 - Playback of the next message begins.
 - The LED flashes during this entire process.
- d) If the device is currently playing a message that is the last one:
- Playback is halted.
 - The playback pointer is advanced to the first message.
 - If present, SE2 is played.
 - Playback of the first message begins.
 - The LED flashes during this entire process.

Triggering of the $\overline{\text{FWD}}$ operation during an erase or record operation is an illegal operation and will be ignored.

8.1.4 Erase Operation

Erasing individual message takes place only if the playback pointer is at either the first or the last message. Erasing individual messages other than the first or last message is not possible. However, global erase can be executed at any message location and will erase all messages. These two erase modes are characterized as follows:

- a) **Individual Erase:** Only the first or last messages can be individually erased. Pulsing $\overline{\text{ERASE}}$ Low performs actions dependent upon the current location of the playback pointer:
- If the device is idle and the playback pointer is currently pointing to the first message:
 - First message is erased.
 - SE2, if present, will be played and the LED will flash twice.
 - Playback pointer will be updated to point to the new first message (previously, the second message).
 - If the device is idle and the playback pointer is currently pointing to the last message:
 - Last message is erased.
 - SE2, if present, will be played and the LED will flash twice.
 - Playback pointer will be updated to point to the new last message (previously, the second to last message).
 - If the device is idle and the playback pointer is *not* currently pointing to the first or last message:
 - No message is erased.
 - SE3, if present, will be played and the LED will flash twice.
 - Play pointer will be unchanged.

ISD1700 SERIES



- If the device is currently playing the first or last message, pressing $\overline{\text{ERASE}}$ will delete the current message, as in the related cases described above.
- b) **Global Erase:** Level-triggering $\overline{\text{ERASE}}$ at Low for more than 2.5 seconds initiates the Global Erase operation and deletes all messages, except the Sound Effects (SEs). See the below figure for operation details. The $\overline{\text{ERASE}}$ is debounced internally.
- If SEs are not recorded:
 - Then no SEs will be played. Nevertheless, the entire erase operation can still be observed via the LED output, if an LED is connected appropriately.
 - The device will blink LED twice once $\overline{\text{ERASE}}$ is triggered to indicate the current message being erased if it is either the first or last one.
 - If $\overline{\text{ERASE}}$ is kept Low constantly, the LED will be blinked seven times to indicate all messages being erased. However, if $\overline{\text{ERASE}}$ is released before the first three blinks of LED, then global erase operation will be abandoned. Otherwise, the global erase operation will be performed.
 - If SEs are present:
 - The device will play SE2 once $\overline{\text{ERASE}}$ is triggered.
 - The device will play SE1 three times after $\overline{\text{ERASE}}$ continues to be held Low for 2.5 seconds or more.
 - If $\overline{\text{ERASE}}$ is kept Low continuously, all messages will be erased, and the chip will play SE4 upon completion. However, if $\overline{\text{ERASE}}$ is released during the playback of SE1, then global erase operation will be abandoned. During the entire erase operation, LED will blink accordingly.

Triggering $\overline{\text{ERASE}}$ for individual erase during a record or forward operation is an illegal operation and will be ignored. However, triggering $\overline{\text{ERASE}}$ for an individual erase operation during playback will delete the current played message, if it is the first or last one.

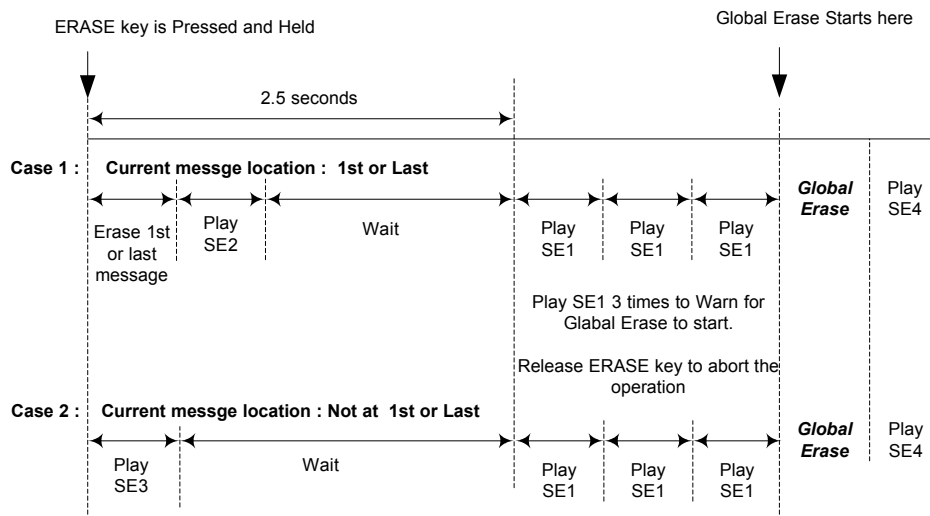


Figure 8.1: Global Erase Operation

ISD1700 SERIES



8.1.5 Reset Operation

A 0.1 μ F capacitor is recommended to connect $\overline{\text{RESET}}$ to ground if a push button switch is used on this pin. When $\overline{\text{RESET}}$ is triggered, the device will place both the record and the playback pointers at the last message. When a microcontroller is used for a power-on-Reset, $\overline{\text{RESET}}$ must stay active for at least 1 μ sec after all supply rails reach their proper specifications.

8.1.6 VOL Operation

Pulsing $\overline{\text{VOL}}$ Low changes the volume output. Each pulse on $\overline{\text{VOL}}$ will decrease the volume until the minimum setting is reached. Subsequent pulses will increase the volume until the maximum level is reached and the cycle will start again. There are 8 steps of volume control. Each step changes the volume by 4 dB. The $\overline{\text{VOL}}$ is debounced internally. A $\overline{\text{RESET}}$ operation will re-initialize the volume level to the default state, which is the maximum level.

8.1.7 FT (Feed-Through) Operation

The $\overline{\text{FT}}$ controls the feed-through path from the input to the output of the chip. When $\overline{\text{FT}}$ is held Low, FT mode is enabled. By factory default, FT mode will pass Analn to SPK and AUD outputs if the device is idle. It will record Analn to the memory during a record operation.

However, the FT path is subject to the contents of NVCFG register during power-on-reset. Once power-up, one can change the setting of the APC register using the related SPI commands.

8.2 vALERT FEATURE (OPTIONAL)

If this optional feature is enabled, after a recording operation, the LED output will blink once every few seconds to indicate the presence of a new message, while the device is in power-down state. After any subsequent operations which power-up the device, the vAlert will stop flashing.

8.3 SOUND EFFECT (SE) EDITING

SE editing can be accessed via push buttons. The first sixteen addresses are shared equally by four Sound Effects (SE1, SE2, SE3, and SE4).

8.3.1 Sound Effects (SEs)

The functions of SEs are as follows:

- SE1: Beginning of recording, forward or global erase warning
- SE2: End of recording, single erase or forward from last message
- SE3: Invalid operation
- SE4: Global erase

ISD1700 SERIES



Whether or not the SEs are programmed, the LED will flash accordingly. The LED flashes once for SE1, twice for SE2, and so on. The frequency of flashing depends upon the sampling frequency selected and the power supply level used.

8.3.2 Entering SE Mode

- First press and hold $\overline{\text{FWD}}$ Low for more than 3 seconds. This action on $\overline{\text{FWD}}$ will play SE1 and cause the LED to blink once (if at the last message location, the chip will play SE2 and the LED will blink twice).
- While holding $\overline{\text{FWD}}$ Low, press and hold the $\overline{\text{REC}}$ Low until the LED blinks once. The device is now in SE editing mode.
- The LED flashing once indicates that SE1 is accessible.

8.3.3 SE Editing

- When in SE editing mode, one can perform record, play, or erase operation on each SE by pressing the appropriate button. For example, to record SE, simply press and hold $\overline{\text{REC}}$. Similarly for play and erase functions, press and hold $\overline{\text{PLAY}}$ or $\overline{\text{ERASE}}$, respectively.
- A $\overline{\text{FWD}}$ operation moves the record and playback pointers to the next SE sequentially. The LED will blink 1~4 times after such operations to indicate which SE is active. If $\overline{\text{FWD}}$ is pressed while accessing SE4, the LED will flash once to indicate that SE1 is again active.
- While the LED is blinking, the device will ignore any input commands. The User must wait until the LED stops blinking before any record, play or erase command can be sent.

8.3.4 Exiting SE Mode

- First press and hold $\overline{\text{FWD}}$ until the LED stops blinking. Then, simultaneously press and hold the $\overline{\text{REC}}$ Low until the LED blinks twice and SE2 (if present) is played. The device has now exited from SE editing mode.

8.3.5 Sound Effect Duration

The duration of sound effects is determined by the sampling frequency selected. All sound effects with the same sampling frequency have the same duration.

Table 8.1 Sound Effect Duration vs. Sampling Frequency

Sampling Frequency	12 kHz	8 kHz	6.4 kHz	5.3 kHz	4 kHz
Duration of SE	0.33 sec	0.5 sec	0.625 sec	0.75 sec	1 sec

8.4 ANALOG INPUTS

ISD1700 SERIES



8.4.1 Microphone Input

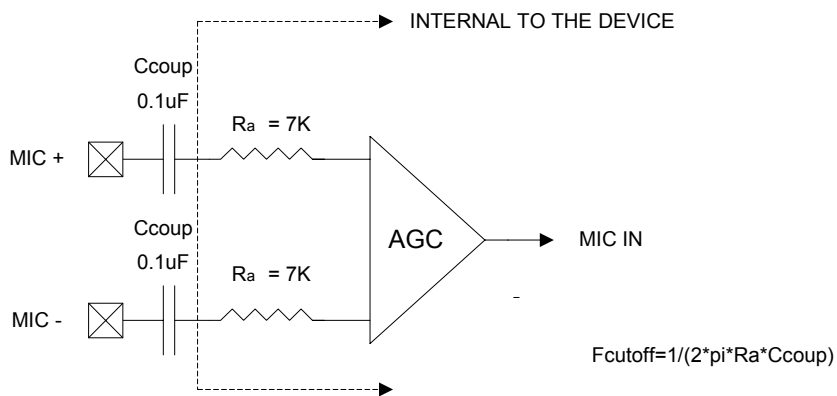


Figure 8.2: MIC input impedance (When this path is active)

8.4.2 Analn Input

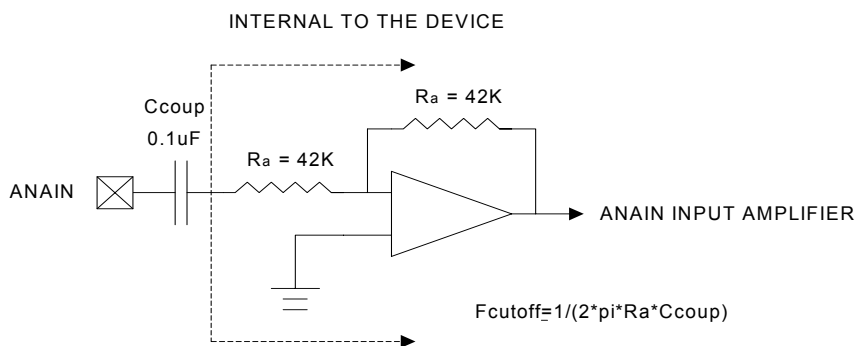


Figure 8.3: Analn input impedance (When the device is powered-up)



9 CIRCULAR MEMORY MANAGEMENT

The ISD1700 has a built-in circular memory management protocol to handle message management internally in Standalone mode. Before the device attempts to access memory via push-button controls or the SPI equivalent commands, it checks the memory structure for conformity to this circular memory protocol. If it fails, the LED will flash seven times and the device accepts no commands except reset and global erase in standalone mode. The only way to recover from this condition is to perform global erase function.

The area of memory under circular memory management control is from address 0x010 to the end of memory, i.e only for the voice message storage. This is because the first sixteen rows, up to address 0x00F are reserved for sound effects (SE). When the address pointer reaches the end of the memory, it will automatically roll over to address 0x010. To comply to the circular memory management protocol, all messages must form a contiguous block and there must be at least one blank row left between the last message and first message. This allows ISD1700 state machine to find the first and last message in memory after POR or Chk_Mem in SPI mode. This circular message management is automatically implemented by the ISD1700 in standalone mode and the similar push-button SPI commands.

In SPI mode, however, the user has the option of direct addressing the array with the SET_PLAY, SET_REC and SET_ERASE commands, which are capable of going around this structure. This may be advantageous if the user wishes to implement a fragmented memory management scheme externally to the ISD1700. These SET commands also permit the recording, playback and erasing the sound effects in SPI mode. The SET_PLAY command can never corrupt the circular memory protocol. The SET_REC and SET_ERASE have the ability to fragment the message memory and invalidate the circular memory structure. Thus, if standalone operation or internal memory management is required, care must be taken in using these commands while in SPI mode.

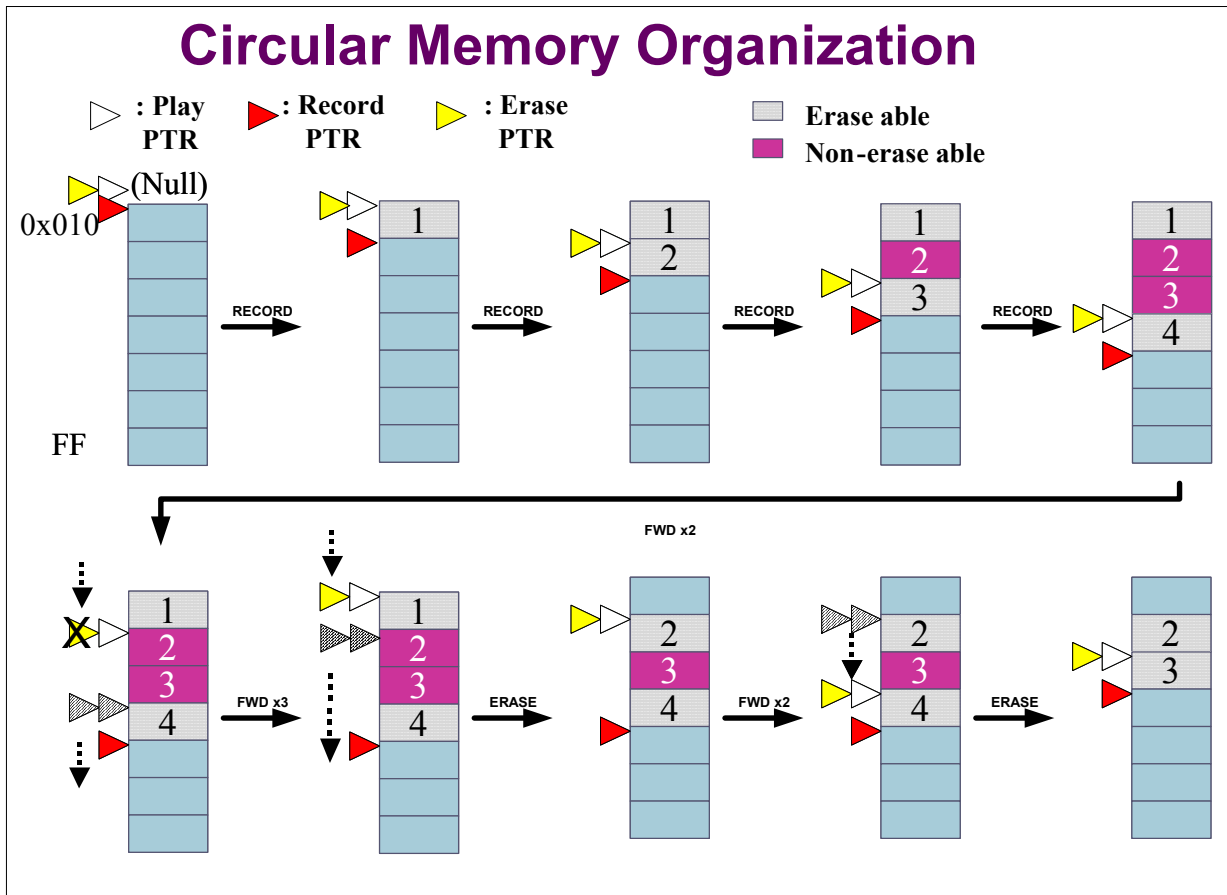


Figure 9.1 Circular Memory Management

An example of the Circular memory management is shown in Figure 9.1. Here the memory array starts from an empty state, the ISD1700 detects this and sets the record pointer to point at row 0x010, the first row of normal memory. A subsequent REC command will record message 1. Now the play pointer will point to the beginning of message 1 and the record pointer to the next row after message 1. Three more recordings will write message 2, 3 and 4. This results the record and play pointers are at next row after message 4 and beginning of message 4, respectively. If two FWD commands are now sent, the play pointer will jump from last message to message 1 then message 2. Note that the erase pointer is now invalid since erase is restricted to only the first or last message. If three FWD commands were executed, the play pointer would end up back at message 1 after wrapping around the last message. Because the pointer is at the first message an erase command is valid. An ERASE will remove message 1 from the memory. Note that the record pointer has been unaffected by all these operations. A further two FWD and a subsequent ERASE commands will remove message 4.

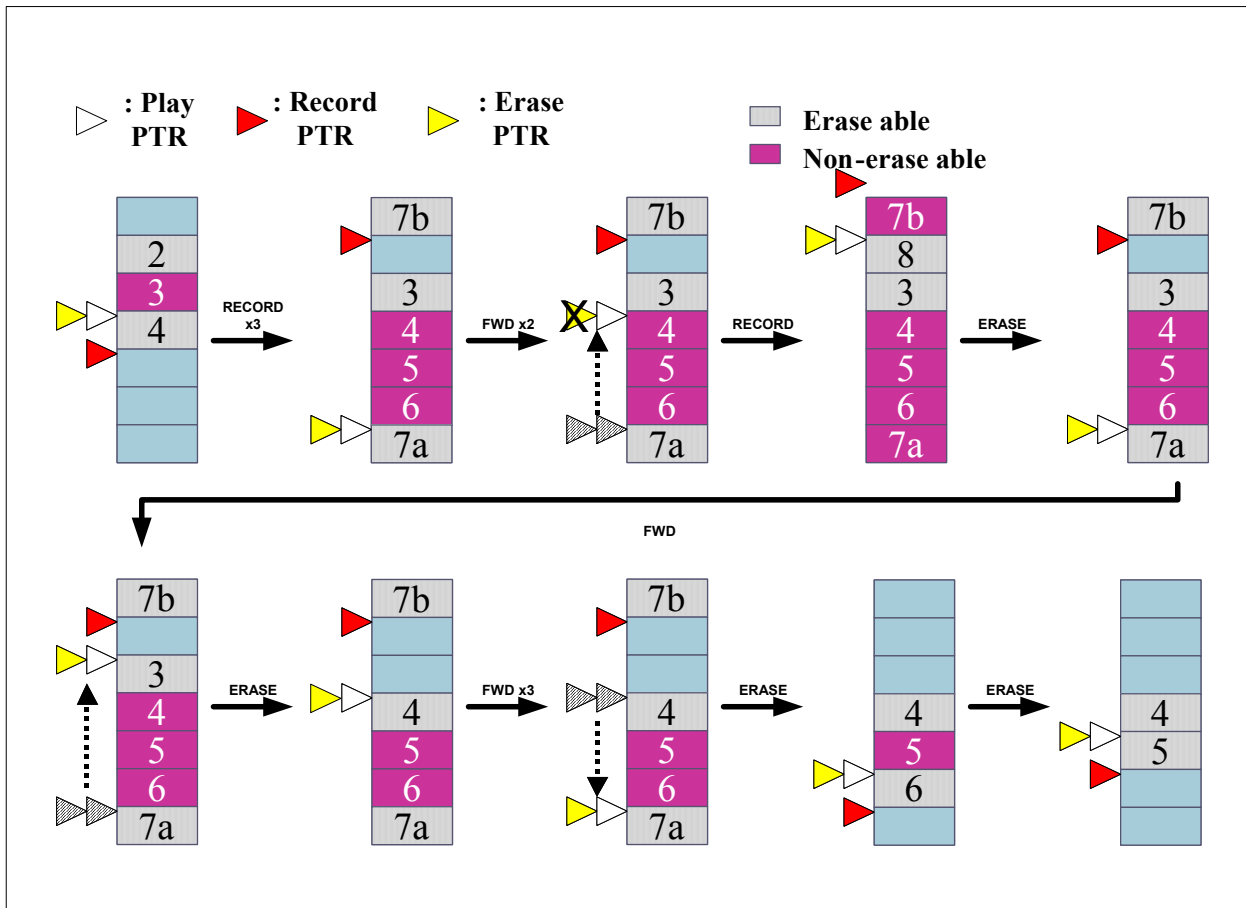


Figure 9.2 Further Circular Message Management

A Further example of circular memory management is shown in Figure 9.2. Here note how the three REC commands cause message 7 to be split across the end of memory boundary. Two FWD commands will wrap the play pointer to message four – the second message in the circular queue. Now if we record until the memory is full, the record pointer becomes invalid and no further record commands will be accepted by the device. Either the first or last message must be erased first. The example above demonstrates erasing the last and then the first message as well.

9.1 RESTORING CIRCULAR MEMORY ARCHITECTURE

In case the circular memory architecture is broken, the LED will blink seven times when either **REC**, **PLAY**, **ERASE** or **FWD** button or alike SPI commands are activated. During such occurrence, the only way to recover back to an operating status is to perform a global erase operation successfully. In order to perform this effectively, one has to press-and-hold the **ERASE** for approximately twelve seconds (time for LED to blink seven times plus period for global erase) at 8 kHz sampling frequency. As a result, the device will resume back to the normal condition.



10 SERIAL PERIPHERAL INTERFACE (SPI) MODE

10.1 MICROCONTROLLER INTERFACE

A four-wire (SCLK, MOSI, MISO & \overline{SS}) SPI interface may be used for serial communication to the ISD1700 device. The ISD1700 Series is configured to operate as a peripheral slave device. All operations may be controlled through this SPI interface.

To allow compatibility with Standalone mode, some SPI commands: PLAY, REC, ERASE, FWD, RESET and G_ERASE behave similarly as the corresponding features in Standalone mode. In addition, SET_PLAY, SET_REC and SET_ERASE commands allow the user to specify the start and the end address of the operation. Besides, there are commands accessing the APC register which controls the configuration of the analog paths used by the device.

10.2 SPI INTERFACE OVERVIEW

The ISD1700 series operates via the SPI serial interface with the following protocol.

Data transfer protocol requires that the microcontroller's SPI shift registers are clocked out on the falling edge of the SCLK. The SPI protocol of the ISD1700 device is as follows:

1. A SPI transaction is initiated on the falling edge of the \overline{SS} pin.
2. \overline{SS} is held low during the entire data transfer process.
3. Data is clocked into the device through the MOSI pin on the rising edge of the SCLK signal and clocked out of the MISO pin on the falling edge of the SCLK signal, with LSB first.
4. The opcodes contain command, data and address bytes, depending upon the command type.
5. The status register and current row address are shifted out of the MISO pin, while control and address data are simultaneously shifted into the MOSI pin.
6. The SPI transaction is completed by raising \overline{SS} high.
7. After completing an operational SPI command, an active low interrupt is generated. It will stay low until it is reset by the CLR_INT command.

10.2.1 SPI Transaction Format

Figure 10.1 describes the format of the SPI transaction. Data is shifted into the device on the MOSI data line. The first byte shifted in is the command byte. This opcode determines what, if any, data is to follow. Concurrently, the device status and current row address is returned to the host via the MISO data line.

ISD1700 SERIES

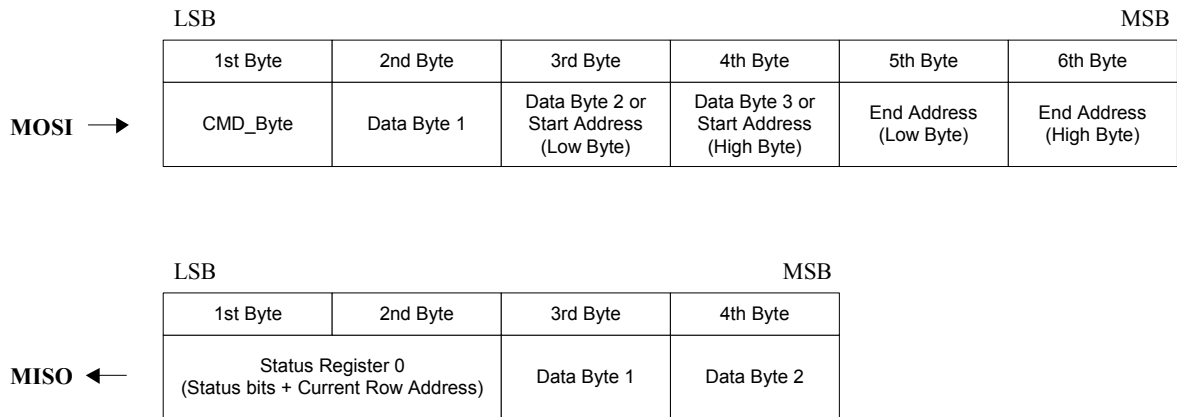


Figure 10.1 SPI Transaction Format

10.2.2 MOSI Data Format

MOSI is the **Master Out Slave In** data line of the SPI interface. Data is clocked into the device on the rising edge of the SCLK signal, with the least significant bit (LSB) first. Depending upon the command type, the format may be two byte or as long as seven bytes. The generalized sequence of MOSI data is shown in the table below. The first byte sent to the device is the command opcode byte which determines the operation that the device is going to perform. Bit 4 (C4) of the command byte determines whether the LED feature is activated for related operations. When C4=1, the LED is On. Subsequent bytes are data associated with the command and may include start and end addresses for operation on the memory array or other data bits.

Table 10.1 MOSI Data Sequence

MSB 1 st Byte: Command Byte LSB							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
C7	C6	C5	C4	C3	C2	C1	C0
MSB 2 nd Byte: Data Byte 1 LSB							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
D7	D6	D5	D4	D3	D2	D1	D0
MSB 3 rd Byte: Data Byte 2 / Start Address (Low Byte) LSB							
Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
X/S7	X/S6	X/S5	X/S4	X/S3	D10/S2	D9/S1	D8/S0
MSB 4 th Byte: Data Byte 3 / Start Address (High Byte) LSB							
Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
X	X	X	X	X	S10	S9	S8
MSB 5 th Byte: End Address (Low Byte) LSB							

ISD1700 SERIES



Bit 39	Bit 38	Bit 37	Bit 36	Bit 35	Bit 34	Bit 33	Bit 32
E7	E6	E5	E4	E3	E2	E1	E0
MSB 6th Byte: End Address (Mid Byte) LSB							
Bit 47	Bit 46	Bit 45	Bit 44	Bit 43	Bit 42	Bit 41	Bit 40
0	0	0	0	0	E10	E9	E8
MSB 7th Byte: End Address (High Byte) LSB							
Bit 55	Bit 4654	Bit 53	Bit 52	Bit 51	Bit 50	Bit 49	Bit 48
0	0	0	0	0	0	0	0

Note: X = Don't care (Recommend 0)

The majority of commands are two byte commands. Commands that require addresses are seven bytes. The LD_APC command is three bytes, in which the 2nd and 3rd bytes are data.

There are two sets of 11 address bits, either <S10:S0> or <E10:E0>, reserved for address locations. They are in binary format as specified above. Address count starts at address 0x000, which is the start location of the first SE. Address locations 0x000-0x00F inclusively are reserved equally for 4 sound effects. Address 0x010 is the first address of non-reserved storage. For minimum storage resolution, please refer to Section 6.2.

10.2.3 MISO Data Format

Data is clocked out of the **Master In Slave Out** pin of ISD1700 device on the falling edge of the SCLK signal, with LSB first. MISO returns the status generated by the last command and current row address <A10:A0> in the first two bytes for all operations. The commands RD_STATUS, RD_PLAY_PNTR, RD_REC_PNTR and RD_APC provide additional information in the subsequent bytes (see below sections for more details). The sequence of MOSI is shown in the table below.

Table 10.2 MISO Data Sequence

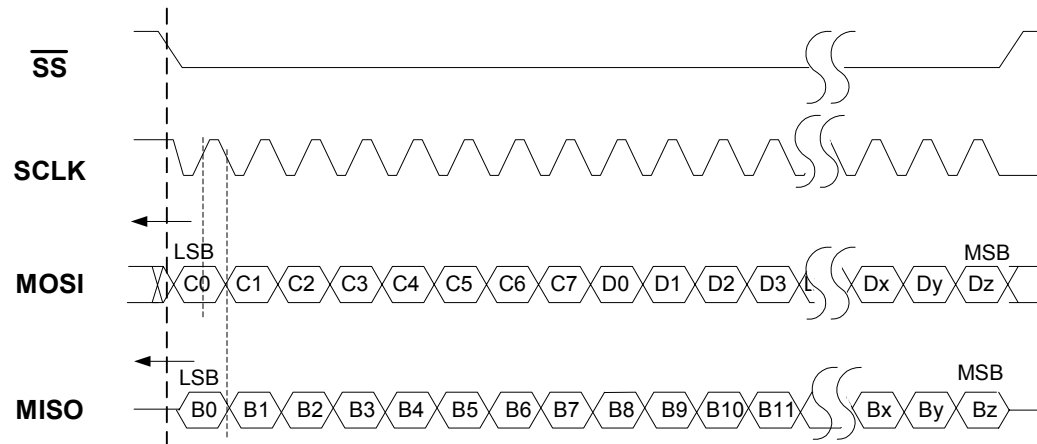
LSB 1st Byte : Status Register 0 MSB							
Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
CMD_Err	Memory Full	Power Up	EOM	Interrupt	A0	A1	A2
LSB 2nd Byte : Status Register 0 MSB							
Bit 8	Bit 9	Bit 10	Bit 11	Bit 12	Bit 13	Bit 14	Bit 15
A3	A4	A5	A6	A7	A8	A9	A10
LSB 3rd Byte : Data Byte 1 MSB							
Bit 16	Bit 17	Bit 18	Bit 19	Bit 20	Bit 21	Bit 22	Bit 23
D0	D1	D2	D3	D4	D5	D6	D7
LSB 4th Byte : Data Byte 2 MSB							
Bit 24	Bit 25	Bit 26	Bit 27	Bit 28	Bit 29	Bit 30	Bit 31
D8	D9	D10	D11	D12	D13	D14	D15

ISD1700 SERIES



The status bits of the 1st byte provide important information on the result of the previous command sent. In particular, bit 0 (command error bit) indicates whether the chip is able to process the previous command or not. The address bits <A10:A0> represent the address location. The contents of the Data Bytes 1 & 2 are depended upon the previous command.

SPI Format



where D_n represents input data bit of MOSI, while B_n are output data bit.

The initial condition of the SPI inputs to the ISD1700 should be:

- \overline{SS} = High
- SCLK = High
- MOSI = Low

10.3 SPI COMMAND OVERVIEW

The SPI commands offer greater control over the device than that in standalone mode. There are several types of commands:-

- Priority commands:
 - Accepted at any time and do not require state machine intervention.
 - PU, STOP, PD, RD_STATUS, CLR_INT, DEVID, RESET
- Circular memory commands:
 - Execute operations similar to in Standalone mode.
 - PLAY, REC, FWD, ERASE, G_ERASE, RD_REC_PTR, RD_PLAY_PTR
- Analog configuration commands:
 - Enable/disable various configuration paths, load/write APC and NVCFG registers, etc.
 - RD_APC, WR_APC, WR_NVCFG, LD_NVCFG, CHK_MEM,
- Direct memory access commands:
 - Execute operations with start and end addresses.
 - SET_ERASE, SET_REC, SET_PLAY

ISD1700 SERIES



An SPI command always consists of an opcode or command byte. The command byte has one special purpose bit, bit 4 (LED). This bit controls the operation of the LED output. If the user wishes to enable the operation of the LED, all opcodes should have this bit set to 1.

In SPI mode, the memory location is row addressable. The microcontroller (μ C) can access any rows including the reserved Sound Effect rows (0x000-0x00F). The SET_PLAY, SET_REC, and SET_ERASE commands require a start address and an end address specified. If start address and end address are the same, ISD1700 will perform the operation on that row only. The SET_REC will write an EOM marker at the end address. The SET_ERASE will erase all rows specified by start address and end address inclusively.

Additionally, SET_PLAY, SET_REC, and SET_ERASE commands have a one deep FIFO buffer to offer seamless transitions from one block of memory to the next. For example, by sending two consecutive SET_PLAY commands, with two different pairs of address, the μ C can concatenate the playback of two memory blocks without pause or interruption. The RDY bit in Status Register 1 will indicate when the chip is ready to accept the second command. Interrupt will be issued when the operation is completed.

The one deep FIFO buffer is only available for same type of SET commands, i.e. SET_PLAY followed by SET_ERASE will not utilize the buffer and a command error will be generated. As an example, if two consecutive SET-PLAY commands are sent correctly, when the buffer is full and the 1st SET_PLAY operation has encountered an EOM, it will normally ignore the EOM marker. Then the second pair of addresses will be loaded and the chip will jump to the start address of second address pair without reaching the end address of first address pair. This action will eliminate the potential dead time between two recorded blocks.

If circular memory architecture is satisfied, one can use PLAY, REC, FWD, RESET, ERASE and G_ERASE commands, which will function similarly as the REC, PLAY, FWD, RESET, ERASE and global-erase in standalone mode, respectively. These commands will ensure that memory organization remain compatible with standalone operations. However, sound effects will not be activated like in standalone mode. If user wishes to switch between SPI and standalone modes, care must be taken in using SET_REC and SET_ERASE to follow the circular memory architecture.

10.4 SWITCHING FROM SPI MODE TO STANDALONE MODE

While doing so, the following precautions have to be taken into account due to the circular memory architecture. First, the arrangement of messages created in SPI mode must match the circular memory structure. Second, only one empty slot is allowed inside the memory array. Third, the device must be "Reset" either before or after exiting the SPI mode, prior to any user mode functions being performed. Failure to do so will cause malfunctioning in standalone mode. As a result, LED will flash seven times.

10.5 ISD1700 DEVICE REGISTERS

There are several registers returning the internal state of the ISD1700 device. The following describes each and its access mode.

ISD1700 SERIES



10.5.1 Status Register 0 (SR0)

SR0 is a two bytes data returning from MISO, which includes 5 status bits (D4:D0) and 11 address bits (A10:A0).

SR0		Size:	16 bits			Type:	Read			
Byte #1	Bit # :	D7	D6	D5	D4	D3	D2	D1	D0	
	Name :	A2	A1	A0	INT	EOM	PU	FULL	CMD_ERR	
Byte #2	Bit # :	D15	D14	D13	D12	D11	D10	D9	D8	
	Name :	A10	A9	A8	A7	A6	A5	A4	A3	
Description:		Device status register								
Access		Every SPI command returns SR0 as first two bytes in MISO								

Table 10.3 Bit description of Status Register 0

SR0			
	Bit	Name	Description
Byte #1	7	A2	Current row address bit 2
	6	A1	Current row address bit 1
	5	A0	Current row address bit 0
	4	INT	This bit is set to 1 when current operation is done. It can be cleared by CLR_INT command.
	3	EOM	This bit is set to 1 when an EOM is detected. It can be cleared by CLR_INT command.
	2	PU	This bit is set to 1 when the device is powered up and operating in SPI mode.
	1	FULL	This bit, when set to 1, indicates memory array is full. That means the device cannot record any new messages unless old messages are deleted. This bit is only valid when user follows push button format to program and erase the array.
	0	CMD_ERR	This bit indicates the previous SPI command is invalid when is set to 1, if: μ C sends less than 5 bytes of row address, SPI command is decoded but ignored.
Byte #2	15	A10	Current row address bit 10
	14	A9	Current row address bit 9
	13	A8	Current row address bit 8
	12	A7	Current row address bit 7
	11	A6	Current row address bit 6
	10	A5	Current row address bit 5
	9	A4	Current row address bit 4
	8	A3	Current row address bit 3

where <A10:A0> is the active row of memory

ISD1700 SERIES



10.5.2 Status Register 1 (SR1)

SR1	Size:	8 bits	Type:	Read				
Bit Sequence:	D7	D6	D5	D4	D3	D2	D1	D0
	SE4	SE3	SE2	SE1	REC	PLAY	ERASE	RDY
Description:	Device secondary status register							
Access	RD_STATUS command. <D7:D0> is the third byte of MISO							

Table 10.4 Bit description of Status Register 1

SR1		
Bit	Name	Description
7	SE1	This bit is set to 1 when sound effect 1 is recorded and 0 when erased
6	SE2	This bit is set to 1 when sound effect 2 is recorded and 0 when erased
5	SE3	This bit is set to 1 when sound effect 3 is recorded and 0 when erased
4	SE4	This bit is set to 1 when sound effect 4 is recorded and 0 when erased
3	REC	This bit (=1) indicates current operation is recording
2	PLAY	This bit (=1) indicates current operation is playback
1	ERASE	This bit (=1) indicates current operation is erase
0	RDY	<p>In SPI mode, SPI is ready to accept new command, if this bit equals to 1. For REC, PLAY or ERASE, if RDY=0 means the device is busy and will not accept a new command, except RESET, CLR_INT, RD_STATUS, PD. REC and PLAY will also accept STOP command. If other commands are sent, it will be ignored and CMD_ERR will set to 1.</p> <p>For any SET commands, RDY=1 means the buffer is empty, SPI can accept similar SET command. If host sends other commands, SPI will ignore it and set CMD_ERR to 1 unless new commands are RESET, CLR_INT, RD_STATUS, and PD. SET_REC and SET_PLAY will also accept STOP command.</p> <p>In standalone mode, RDY=0 indicates the device is busy.</p>

10.5.3 APC Register

APC	Size:	12 bits	Type:	R/W
Bit Sequence:	<D11:D0> (See Table 7.1)			
Description:	Analog Path Configuration register.			
Access	Read: RD_APC; Write: LD_APC			

10.5.4 Play Pointer

PLAY_POINTER	Size:	11 bits	Type:	Read
Bit Sequence:	PLAY_POINTER <A10:A0>			

ISD1700 SERIES



Description:	Pointer at beginning of current message for circular memory management.
Access	Read: RD_PLAY_PTR; Changed by FWD, RESET

10.5.5 Record Pointer

REC_POINTER	Size:	11 bits	Type:	Read
Bit Sequence:	REC_POINTER<A10:A0>			
Description:	Pointer at first available row in circular memory.			
Access	Read: RD_REC_PTR; Changed by REC			

10.5.6 DEVICEID Register

DEVICEID	Size	8 bits	Type	Read				
Bit Sequence:	D7	D6	D5	D4	D3	D2	D1	D0
	CHIPID					Reserved		
Description:	Device identification register							
Access	DEVID command as third byte of MISO							

Table 10.5 Bit description of DEVICEID Register

DEVICEID			
Bits	Name	Description	
<7:3>	CHIPID	DDDDD 76543	Device
		11100	ISD17240
		11101	ISD17210
		11110	ISD17180
		11000	ISD17150
		11001	ISD17120
		11010	ISD1790
		10100	ISD1760
		10101	ISD1750
		10110	ISD1740
		10000	ISD1730
<2:0>	Reserved	Reserved	

ISD1700 SERIES



11 SPI COMMAND REFERENCE

This section describes the SPI command set. A summary of commands is given in Table 11.1 and commands are detailed in subsequent sub-sections.

Table 11.1 SPI Command Reference

Instruction	Command Byte <C7:C0> ^[1]		CMD_Data_Byte <D7:D0>	Start Addr <xxxxx S10:S0> (2-Byte) ^[2]	End Addr <xxxx xxxx xxxxxE10:E0> (3-Byte) ^[2]	Description
	Hex	Binary cccc cccc 7654 3210				
PU	0x01	0000 0001	0000 0000			Power up the device
STOP	0x02	0000 0010	0000 0000			Stop the current operation
RESET	0x03	0000 0011	0000 0000			Reset the device
CLR_INT	0x04	0000 0100	0000 0000			Clear interrupt and EOM bit
RD_STATUS	0x05	0000 0101	0000 0000	0000 0000		Returns status bits & current row counter in first 1 st 2 bytes and operating status in 3 rd byte
RD_PLAY_PTR	0x06	0000 0110	0000 0000	0000 0000 0000 0000		Returns status bits & current row counter in 1 st 2 bytes and Play pointer in 3 rd & 4 th bytes
PD	0x07	0000 0111	0000 0000			Power down the device
RD_REC_PTR	0x08	0000 1000	0000 0000	0000 0000 0000 0000		Returns status bits & current row counter in 1 st 2 bytes and Record pointer in 3 rd & 4 th bytes
DEVID	0x09	0000 1001	0000 0000	0000 0000		Read the device ID register.
PLAY	0x40	0100 0000	0000 0000			Play from current location without LED action until EOM or STOP command received
REC	0x41	0100 0001	0000 0000			Record from current location without LED action until end of memory or STOP command received
ERASE	0x42	0100 0010	0000 0000			Erase current message to EOM location
G_ERASE	0x43	0100 0011	0000 0000			Erase all messages (not include Sound Effects)

ISD1700 SERIES



RD_APC	0x44	0100 0100	0000 0000	0000 0000 0000 0000		Returns status bits & current row counter in first 1 st 2 bytes and the contents of APC register in 3 rd & 4 th bytes.
WR_APC1	0x45	0100 0101	<D7:D0>	<xxxxx D10:D8>		Write the data <D10:D0> into the APC register with volume setting from <u>VOL</u> pin
WR_APC2	0x65	0110 0101	<D7:D0>	<xxxxx D10:D8>		Write the data <D10:D0> into the APC register with volume setting from bits <D2:D0>
WR_NVCFG	0x46	0100 0110	0000 0000			Write the contents of APC to NVCFG
LD_NVCFG	0x47	0100 0111	0000 0000			Load contents of NVCFG to APC Register
FWD	0x48	0100 1000	0000 0000			Forward play pointer to start address of next message. Forward will be ignored during operating, except Play
CHK_MEM	0x49	0100 1001	0000 0000			Check circular memory
EXTCLK	0x4A	0100 1010	0000 0000			Enable/disable external clock mode
SET_PLAY	0x80	1000 0000	0000 0000	<xxxxx S10:S0>	<xxxx xxxx xxxxxE10:E0>	Play from start address <S10:S0> to end address <E10:E0> or stop at EOM, depending on the D11 of APC
SET_REC	0x81	1000 0001	0000 0000	<xxxxx S10:S0>	<xxxx xxxx xxxxxE10:E0>	Record from start address <S10:S0> to end address <E10:E0>
SET_ERASE	0x82	1000 0010	0000 0000	<xxxxx S10:S0>	<xxxx xxxx xxxxxE10:E0>	Erase from start address <S10:S0> to end address <E10:E0> [Stop cmd is ignored]

Note: ^[1] Bit C4 (LED) must be set to 1 if LED indication is required. During the active state of LED output, no new command will be accepted.

^[2] For “xxx...”, recommend to use “000...”

11.1 SPI PRIORITY COMMANDS

This class of SPI commands will always be accepted by the ISD1700. They control power up and down of the device, interrogating the status of the device and clearing interrupt requests.

11.1.1 PU Power Up (0x01)

PU	Opcode:	0x01	0x00	Interrupt:	No	
Byte Sequence:	MOSI		0x01	0x00		
	MISO		SR0			
Description:	Power up					

ISD1700 SERIES



State before Execution	Power Down
State after Execution	Idle/FT
Registers Affected	SR0: PU bit, SR1: RDY bit

This command wakes up the ISD1700 device and make it enter into the SPI idle state. Upon executing this command, PU bit of SR0 and RDY bit of SR1 will be set to 1. This command does not generate an interrupt. Once in SPI mode, the input from \overline{FT} pin will be ignored and its function will be replaced by Bit 6 of the APC register. SPI mode is exited via a PD (power down) command.

11.1.2 STOP (0x02)

STOP	Opcode:	0x02	0x00	Interupt:	Yes	
Byte Sequence:	MOSI		0x02	0x00		
	MISO		SR0			
Description:	Stop the current operation					
State before Execution	REC, PLAY, SET_PLAY, SET_REC					
State after Execution	Idle/FT					
Registers Affected	SR0: INT bit, SR1: RDY/PLAY/REC bits					

This command stops the current operation. It is valid for the operations: PLAY, REC, SET_PLAY and SET_REC. The execution time of the command is dependent upon the active operation. See timing section for stopping various active states.

The CMD_ERR bit of SR0 will be set if the STOP command is sent during ERASE, G_ERASE and SET_ERASE operations. If STOP is sent while the device is idle, no action will be taken and no interrupt generated.

11.1.3 RESET (0x03)

RESET	Opcode:	0x03	0x00	Interupt:	No	
Byte Sequence:	MOSI		0x03	0x00		
	MISO		SR0			
Description:	Reset the Device					
State before Execution	Any, except PD					
State after Execution	PD					
Registers Affected	SR0, SR1, APC					

11.1.4 CLR_INT(0x04)

CLR_INT	Opcode:	0x04	0x00	Interupt:	No	
Byte Sequence:	MOSI		0x04	0x00		
	MISO		SR0			

ISD1700 SERIES



Description:	Read Status and Clear INT
State before Execution	Any
State after Execution	Does not affect state, clears the INT register and pin.
Registers Affected	SR0: INT bit, EOM bit

The Clear Interrupt command reads the status of the device and clears the status of interrupt & EOM bits. As a result, all interrupt & EOM bits are cleared and $\overline{\text{INT}}$ is released.

11.1.5 RD_STATUS (0x05)

RD_STATUS	Opcode:	0x05	0x00	0x00	Interrupt:	No	
Byte Sequence:	MOSI	0x05	0x00	0x00			
	MISO	SR0		SR1			
Description:	Read Status						
State before Execution	Any						
State after Execution	Does not affect state.						
Registers Affected	None						

The Read Status command reads the status of the device. This command has three bytes. See Table 10.3 and Table 10.4 for description of status register bits.

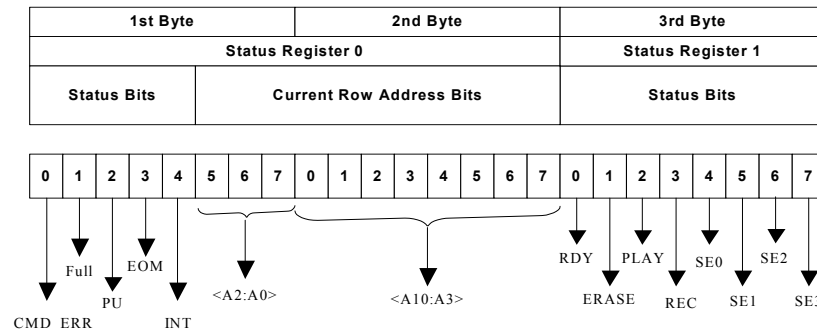


Figure 11.1 Status Read Command

11.1.6 PD (0x07) Power Down

PD	Opcode:	0x07	0x00	Interrupt:	No	
Byte Sequence:	MOSI	0x07	0x00			
	MISO	SR0				
Description:	Power down the device and enter into standby mode					
State before Execution	Any. If sent during a REC, PLAY or ERASE operation, device will finish operation before powering down.					

ISD1700 SERIES



State after Execution	PD
Registers Affected	SR0: PU bit

This command places the ISD1700 into power-down mode. It will also enable standalone mode. If command is sent during an active play/record/erase operation, the device will finish the current operation then power down. Under this condition, the device will generate an interrupt. While exiting SPI mode, the $\overline{\text{INT}}$ /RDY pin status switches from $\overline{\text{INT}}$ to RDY state.

11.1.7 DEVID (0x09) Read Device ID

DEVID	Opcode:	0x09	0x00	Interrupt:	No	
Byte Sequence:	MOSI		0x09	0x00	0x00	
	MISO		SR0		DEVICEID	
Description:	Read the DEVICEID register to identify the device family					
State before Execution	Any					
State after Execution	Does not affect state.					
Registers Affected	None					

The Read Device ID command reads the register that identifies the type of device. This command shows which device in the ISD1700 family is present. This command has three bytes. See Table 10.5 for a description of DEVICEID register bits.

11.2 CIRCULAR MEMORY COMMANDS

A circular memory command performs a simple typical operation similar to the related function as in standalone mode except it does not automatically playback sound effects (SE) for audio feedback of operation. So if sound effect is required, separate command to perform the feature is needed. The commands require that the message address arrangement complies to the circular memory protocol. Before these commands are executed, the ISD1700 checks the memory structure first. If it does not match circular memory structure. then CMD_ERR bit in Status Register 0 (SR0) will be set and command will not execute.

In addition to the push-button similar commands, commands to read the record and play pointers are available to allow the SPI host to track message management and navigate around the circular memory structure.

11.2.1 PLAY (0x40)

PLAY	Opcode:	0x40	0x00	Interrupt:	Yes	
Byte Sequence:	MOSI		0x40	0x00		
	MISO		SR0			
Description:	Device starts to playback from current PLAY_POINTER					
State before Execution	Idle					

ISD1700 SERIES



State after Execution	Playback then Idle
Registers Affected	SR0, SR1: PLAY & RDY bits

The PLAY command starts playback operation from current PLAY_POINTER and stops when it reaches EOM or receives STOP command. During playback, the device will only respond to STOP, RESET, CLR_INT, RD_STATUS and PD commands. CMD_ERR of SR0 is set if other commands are sent. RDY bit of SR1 is Low during PLAY.

11.2.2 REC (0x41)

REC	Opcode:	0x41	0x00	Interrupt:	Yes	
Byte Sequence:	MOSI		0x41	0x00		
	MISO		SR0			
Description:	Device will record from current REC_POINTER					
State before Execution	Idle					
State after Execution	Record then idle					
Registers Affected	SR0, SR1: REC & RDY bits					

The REC command starts record operation from current REC_POINTER and stops when it receives STOP command or memory array is full. Power supply must be remained during the entire operation. In record mode, the device will only respond to STOP, RESET, CLR_INT, RD_STATUS and PD commands. CMD_ERR bit of SR0 is set if other commands are sent. RDY bit of SR1 is Low during recording.

11.2.3 ERASE (0x42)

ERASE	Opcode:	0x42	0x00	Interrupt:	Yes	
Byte Sequence:	MOSI		0x42	0x00		
	MISO		SR0			
Description:	Device will delete the message from current PLAY_POINTER if at first or last message					
State before Execution	Idle					
State after Execution	Erase then idle					
Registers Affected	SR0, SR1: ERASE & RDY bits					

The ERASE command starts erase operation from current PLAY_POINTER if the PLAY_POINTER is at the first or last message. It stops when it reaches EOM. Power supply must be remained during the entire operation. In erase mode, the device will only respond to RESET, CLR_INT, RD_STATUS and PD commands. CMD_ERR bit of SR0 is set if other commands are sent or the PLAY_POINTER is not positioned at the first or last message. RDY bit of SR1 is Low during erase.

11.2.4 G_ERASE (0x43) Global Erase

G_ERASE	Opcode	0x43	0x00	Interrupt	Yes
----------------	--------	------	------	-----------	-----

ISD1700 SERIES



Byte Sequence:	MOSI	0x43	0x00		
	MISO	SR0			
Description:	Device will ERASE all messages.				
State before Execution	Idle				
State after Execution	Erase then idle				
Registers Affected	SR0, SR1: ERASE, RDY				

The G_ERASE command will erase the whole memory array, except the SE portion (row 0x000-0x00F). Upon completion it will generate an interrupt. In G_ERASE mode, the device will only respond to RESET, CLR_INT, RD_STATUS and PD commands. CMD_ERR of SR0 is set if other commands are sent. TheRDY of SR1 is low during erase.

11.2.5 FWD (0x48)

FWD	Opcode	0x48	0x00	Interrupt	Yes	
Byte Sequence:	MOSI	0x48	0x00			
	MISO	SR0				
Description:	Advances the PLAY_POINTER to next message					
State before Execution	IDLE					
State after Execution	IDLE					
Registers Affected	SR0, PLAY_POINTER					

This command causes PLAY POINTER to jump from current address to next START address. Unlike the standalone FWD, FWD will not interrupt a current play operation and can only be issued in the SPI IDLE state. To emulate a standalone FWD command, the STOP command must first be issued, followed by FWD and PLAY. When FWD completes it will generate an interrupt.

To determine where the PLAY_POINTER is in memory the RD_PLAY_POINTER command can be used.

11.2.6 CHK_MEM (0x49) Check Circular Memory

CHK_MEM	Opcode	0x49	0x00	Interrupt	Yes	
Byte Sequence:	MOSI	0x49	0x00			
	MISO	SR0				
Description:	Triggers the device to check circular memory validity					
State before Execution	IDLE					
State after Execution	IDLE					
Registers Affected	SR0, PLAY_POINTER, REC_POINTER					

The CHK_MEM command will cause the device to check that the memory conforms to circular memory protocol. The device must be powered up and in IDLE state for this

ISD1700 SERIES



command to operate. Upon completion, it will generate an interrupt. If CMD_ERR of SR0 is set then memory failed circular memory check. Upon the successful completion of command, the PLAY_POINTER will point to the last message in the line and REC_POINTER will point to the first available memory location.

This command enables the SPI host to interrogate the circular memory structure. After command, the record and play pointers are initialized and can be read to determine the position of the last message. FWD commands can then be sent to access the addresses of the first and subsequent messages.

11.2.7 RD_PLAY_PTR (0x06)

RD_PLAY_PTR	Opcode	0x06	0x00	Interrupt	No
Byte Sequence:	MOSI	0x06	0x00	0x00	0x00
	MISO	SR0		PP<7:0>	xxxxx PP<10:8>
Description:	Will read the current position of the PLAY_POINTER PP<10:0>.				
State before Execution	After CHK_MEM				
State after Execution	No change				
Registers Affected	None				

This command reads out the PLAY_POINTER address. This is the address where a push-button play or PLAY will start from.

11.2.8 RD_REC_PTR (0x08)

RD_REC_PTR	Opcode	0x08	0x00	Interrupt	No
Byte Sequence:	MOSI	0x06	0x00	0x00	0x00
	MISO	SR0		RP<7:0>	xxxxx RP<10:8>
Description:	Will read the current position of the REC_POINTER RP<10:0>.				
State before Execution	After CHK_MEM				
State after Execution	No change				
Registers Affected	None				

RD_REC_PTR reads the REC_POINTER address. This is the first free location in memory for a push-button compatible record. It is where a push-button record or REC will start from.

11.3 ANALOG CONFIGURATION COMMANDS

These commands allow the SPI host to configure the analog properties of the device.

11.3.1 RD_APC (0x44) Read APC Register

RD_APC	Opcode	0x44	0x00	0x00	0x00	Interrupt	No
Byte Sequence:	MOSI	0x44	0x00	0x00	0x00	0x00	
	MISO	SR0		APC<7:0>	xxxxx APC<10:8>		

ISD1700 SERIES



Description:	Will read the current contents of the APC register.
State before Execution	Idle
State after Execution	No change
Registers Affected	None

This command reads out analog path configuration (APC) register. After sending SR0 and current ADDR the ISD1700 will send out the APC register. This command has 4 bytes.

11.3.2 WR_APC1 (0x45) Load APC Register

WR_APC1	Opcode	0x45	D<7:0>	D<10:8>	Interrupt	No	
Byte Sequence:	MOSI	0x45	D<7:0>	xxxxx D<10:8>			
	MISO	SR0		SR0: 1 st byte			
Description:	Will load the data D<10:0> to the APC register with volume setting from $\overline{\text{VOL}}$ pin						
State before Execution	Idle						
State after Execution	No change						
Registers Affected	APC						

The WR_APC1 command loads data to the Analog Path Configuration (APC) Register. There are three bytes in this command. The first byte is command and the second byte has data for APC<7:0> and the third byte contains APC<10:8> as the least significant bits. The five most significant bits of this third byte are ignored. In this command, volume setting is from $\overline{\text{VOL}}$ pin, rather than the bits <D2:D0>. Care must be taken to change only VOL bits if the device is executing an active command otherwise un-intended transients may occur on the analog path.

11.3.3 WR_APC2 (0x65) Load APC Register

WR_APC2	Opcode	0x65	D<7:0>	D<10:8>	Interrupt	No	
Byte Sequence:	MOSI	0x65	D<7:0>	xxxxx D<10:8>			
	MISO	SR0		SR0: 1 st byte			
Description:	Will load the data D<10:0> to the APC register with volume setting from <D2:D0> bits						
State before Execution	Idle						
State after Execution	No change						
Registers Affected	APC						

The WR_APC2 command loads data to the Analog Path Configuration (APC) Register. There are three bytes in this command. The first byte is command and the second byte has data for APC<7:0> and the third byte contains APC<10:8> as the least significant bits. The five most significant bits of this third byte are ignored. In this command, volume setting is from the bits <D2:D0>, rather than $\overline{\text{VOL}}$ pin. Care must be taken to change only VOL bits if the

ISD1700 SERIES



device is executing an active command otherwise un-intended transients may occur on the analog path.

11.3.4 WR_NVCFG (0x46) Write APC to Non-Volatile Memory

WR_NVCFG	Opcode	0x46	0x00	Interrupt	No
Byte Sequence:	MOSI	0x46		0x00	
	MISO	SR0			
Description:	Write the current contents of the APC register into the non-volatile NVCFG register.				
State before Execution	IDLE				
State after Execution	IDLE				
Registers Affected	None				

This command writes data from Analog Path Configuration (APC) register into the non-volatile NVCFG register. This value is loaded to the APC after a power-on condition or RESET. SR0.CMD_ERR is set if ISD1700 is not in IDLE state when this command is sent.

11.3.5 LD_NVCFG (0x47) Load APC register from Non-Volatile Memory

LD_NVCFG	Opcode	0x47	0x00	Interrupt	No
Byte Sequence:	MOSI	0x47		0x00	
	MISO	SR0			
Description:	Load the current non-volatile NVCFG to the APC register.				
State before Execution	IDLE				
State after Execution	IDLE				
Registers Affected	APC				

This command loads the data from the non-volatile register NVCFG into the Analog Path Configuration (APC) register. SR0.CMD_ERR is set if ISD1700 is not in IDLE state when this command is sent.

11.4 DIRECT MEMORY ACCESS COMMANDS

These commands allow the SPI host to access the memory by specifying start and end addresses. For the record and play varieties, the next address pair to operate can be preloaded such that when the operation has finished on the first address pair the operation will seamlessly jump to the next.

All these commands require a START_ADDRESS and END_ADDRESS. They operate from START_ADDRESS to END_ADDRESS inclusive. Because the memory is configured as a circular array, END_ADDRESS < START_ADDRESS is allowed. In this case the ISD1700 will wrap around from the last row of the memory to address 0x010 and continue until END_ADDRESS is reached. Note that care must be taken in accessing the SE rows 0x000-0x00F, if END_ADDRESS < START_ADDRESS and END_ADDRESS < 0x10 then device will loop continuously as END_ADDRESS will never match the current address.

ISD1700 SERIES



11.4.1 SET_PLAY (0x80)

SET_PLAY	Opcode	0x80	0x00	Interrupt	Yes			
Byte Sequence:	MOSI	0x80	0x00	S<7:0>	00000 S<10:8>	E<7:0>	00000 E<10:8>	0x00
	MISO	SR0		SR0		SR0		
Description:	Start a playback operation from start address S<10:0> to end address E<10:0> inclusive or stop at EOM, depending on the D11 of APC.							
State before Execution	Idle							
State after Execution	Play, then idle							
Registers Affected	SR0, SR1:PLAY, RDY							

The SET_PLAY command plays from start address S<10:0> and stops at address E<10:0>. In SET_PLAY mode, the device will only respond to SET_PLAY, STOP, RESET, CLR_INT, RD_STATUS and PD commands. SR0.CMD_ERR is set if other commands are sent. SR1.RDY is low until device has latched addresses and begun playback. If no further command is sent, the device will play until end of row E<10:0>. Once SR1.RDY returns high another SET_PLAY can be sent. The result of this will be to load a second pair of START and END addresses to a buffer. Now when the ISD1700 reaches an EOM in, or the end of, the row of the first end address it will jump to the new start address. At this point SR1.RDY will go low indicating that a new address can be loaded.

11.4.2 SET_REC (0x81)

SET_REC	Opcode	0x81	0x00	Interrupt	Yes			
Byte Sequence:	MOSI	0x81	0x00	S<7:0>	00000 S<10:8>	E<7:0>	00000 E<10:8>	0x00
	MISO	SR0		SR0		SR0		
Description:	Start a record operation from start address S<10:0> to end address E<10:0> inclusive.							
State before Execution	Idle							
State after Execution	Record, then idle							
Registers Affected	SR0, SR1:REC, RDY							

The SET_REC command records from start address S<10:0> and stops at address E<10:0>. In SET_REC mode, the device will only respond to SET_REC, STOP, RESET, CLR_INT, RD_STATUS and PD commands. SR0.CMD_ERR is set if other commands are sent. SR1.RDY is low until device has latched addresses and begun recording. If no further command is sent the device will record until end of row E<10:0> and write an EOM marker there. Once SR1.RDY returns high another SET_REC can be sent. The result of this will be to load a second pair of START and END addresses to a buffer. Now when the ISD1700 reaches the end of row E<10:0> of the first end address it will jump to the new start address, no EOM will be written. At this point SR1.RDY will go low indicating that a new address can be loaded. During the record process, power supply cannot be interrupted. Otherwise, it will cause the device malfunctioned.

ISD1700 SERIES



11.4.3 SET_ERASE (0x82)

SET_ERASE	Opcode	0x82	0x00	Interrupt	Yes			
Byte Sequence:	MOSI	0x82	0x00	S<7:0>	00000 S<10:8>	E<7:0>	00000 E<10:8>	0x00
	MISO	SR0		SR0		SR0		
Description:	Start an erase operation from start address S<10:0> to end address E<10:0> inclusive.							
State before Execution	Idle							
State after Execution	Erase, then idle							
Registers Affected	SR0, SR1:ERASE, RDY							

The SET_ERASE command erases rows from start address S<10:0> and to address E<10:0> inclusive. In SET_ERASE mode, the device will only respond to RESET, CLR_INT, RD_STATUS and PD commands. SR0.CMD_ERR is set if other commands are sent. SR1.RDY is low until device has finished erasing. An INT is generated upon completion of erase operation. During the record process, power supply cannot be interrupted. Otherwise, it will cause the device malfunctioned.

11.5 ADDITIONAL COMMAND

The additional command enhances the functionality and performance of the device in order to fulfill extra features and requirements that the designers wish.

EXTCLK	Opcode	0x4A	0x00	Interrupt	No		
Byte Sequence:	MOSI	0x4A	0x00				
	MISO	SR0					
Description:	Enable or disable the external clock mode						
State before Execution	IDLE						
State after Execution	IDLE						
Registers Affected	None						

The EXTCLK command toggles the enable and disable of the external clock (XCLK) mode on the device. When XCLK mode is activated, the internal oscillator of the device is disabled. Instead, an external clock is required to apply to the Rosc pin and the external resistor at Rosc pin must be removed. When XCLK mode is disabled, then the external clock signal must be disconnected from Rosc pin and an external resistor must be connected back, so that the device runs from its internal clock accordingly. This mode is very useful for exact synchronization of the I1700 device with an external component, say microcontroller, when precision timing is essential. An active XCLK state can also be reset by RESET command or **RESET** control. Hence, the device will operate via its internal oscillator, provided that the external resistor is hooked up to the Rosc pin.

The frequencies of the required external clock with respect to the various sampling frequencies are listed in the below table:

Sampling Freq. [kHz]	12	8	6.4	5.3	4
External Clock Freq. [MHz]	3.072	2.048	1.638	1.356	1.024

ISD1700 SERIES



12 TIMING DIAGRAMS

12.1 RECORD, PLAY AND ERASE

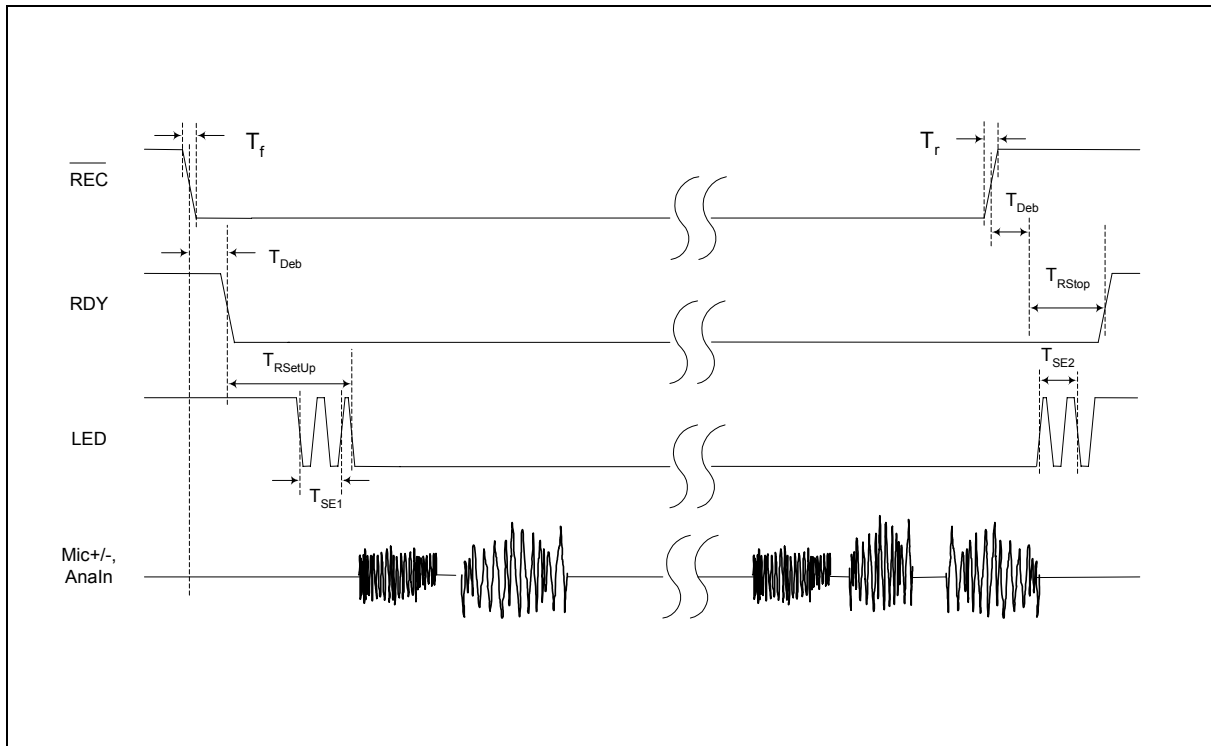


Figure 12.1: Record Operation

ISD1700 SERIES

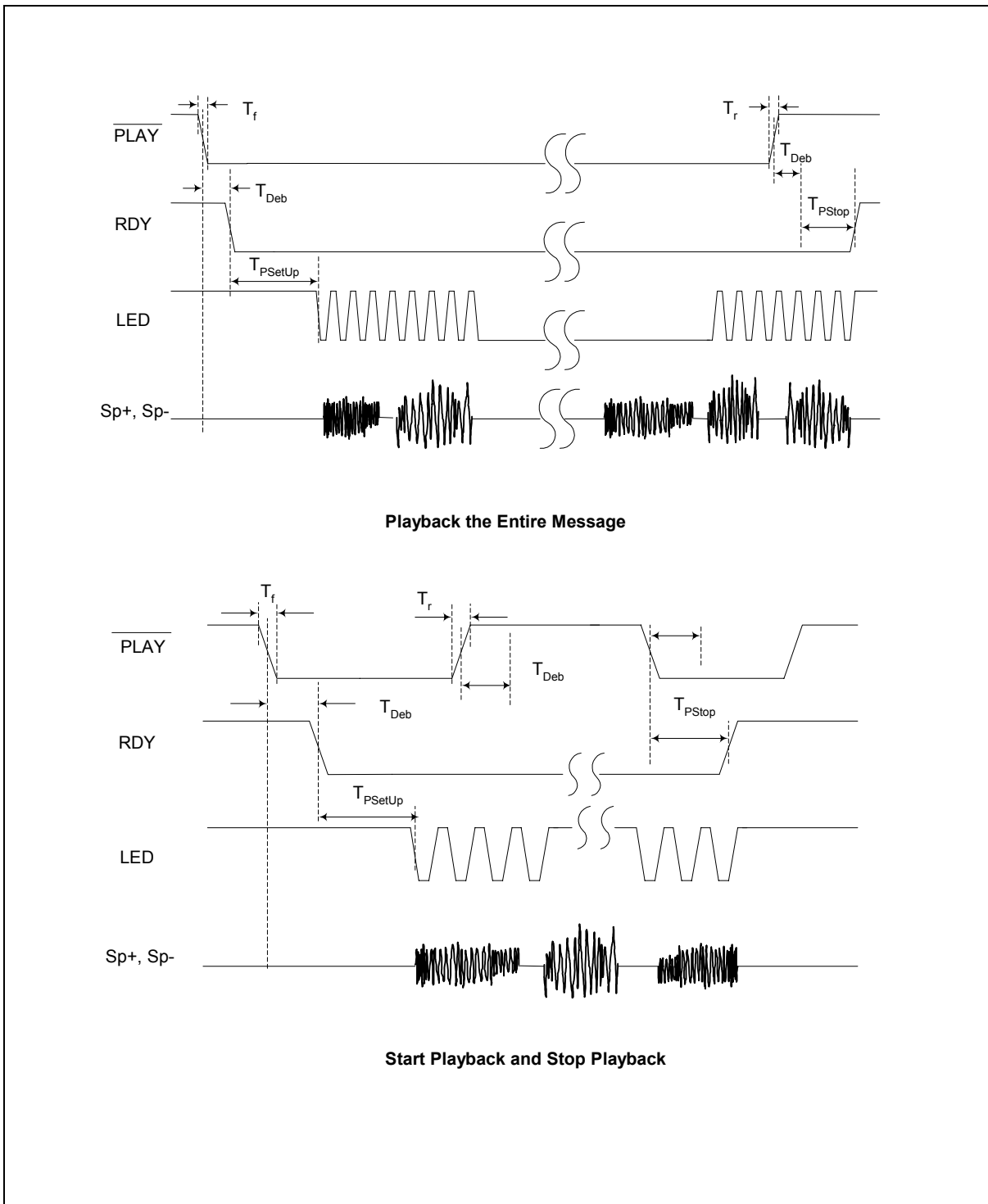


Figure 12.2: Playback Operation

ISD1700 SERIES

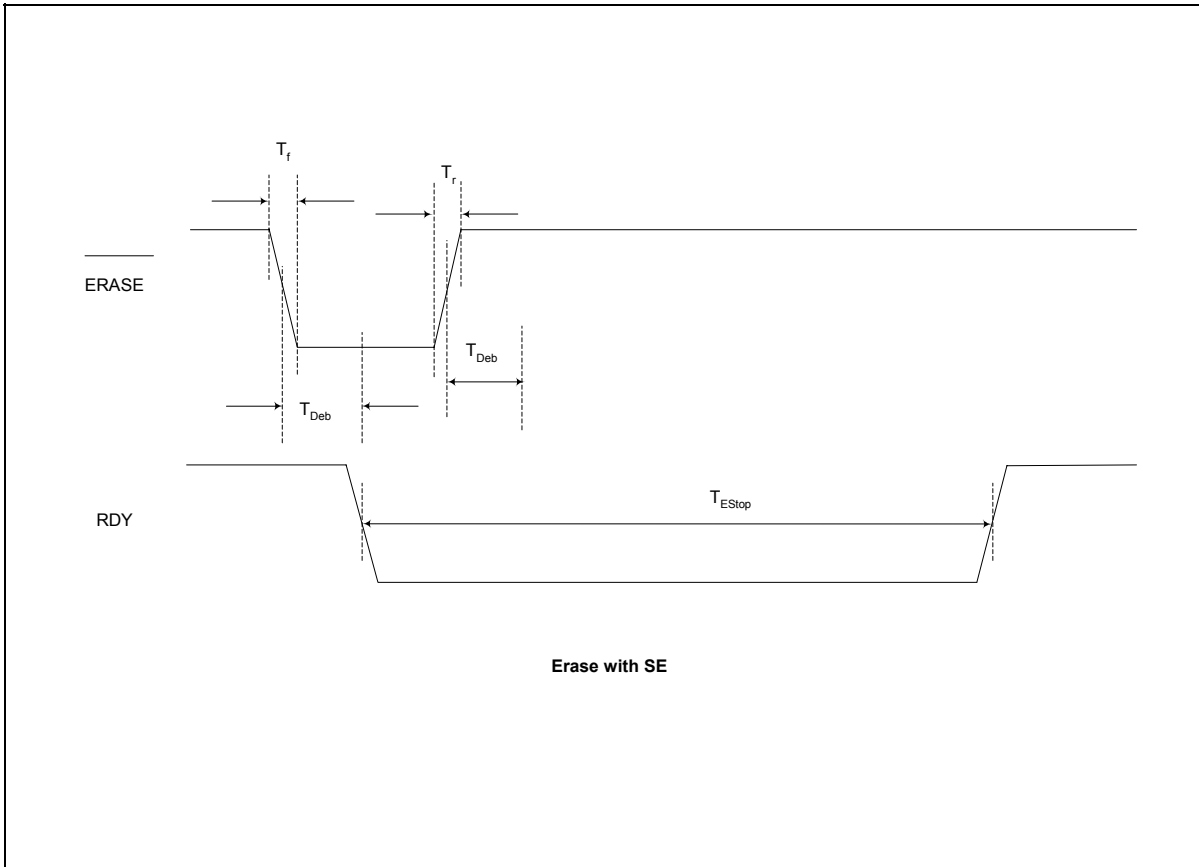


Figure 12.3: Erase Operation

ISD1700 SERIES

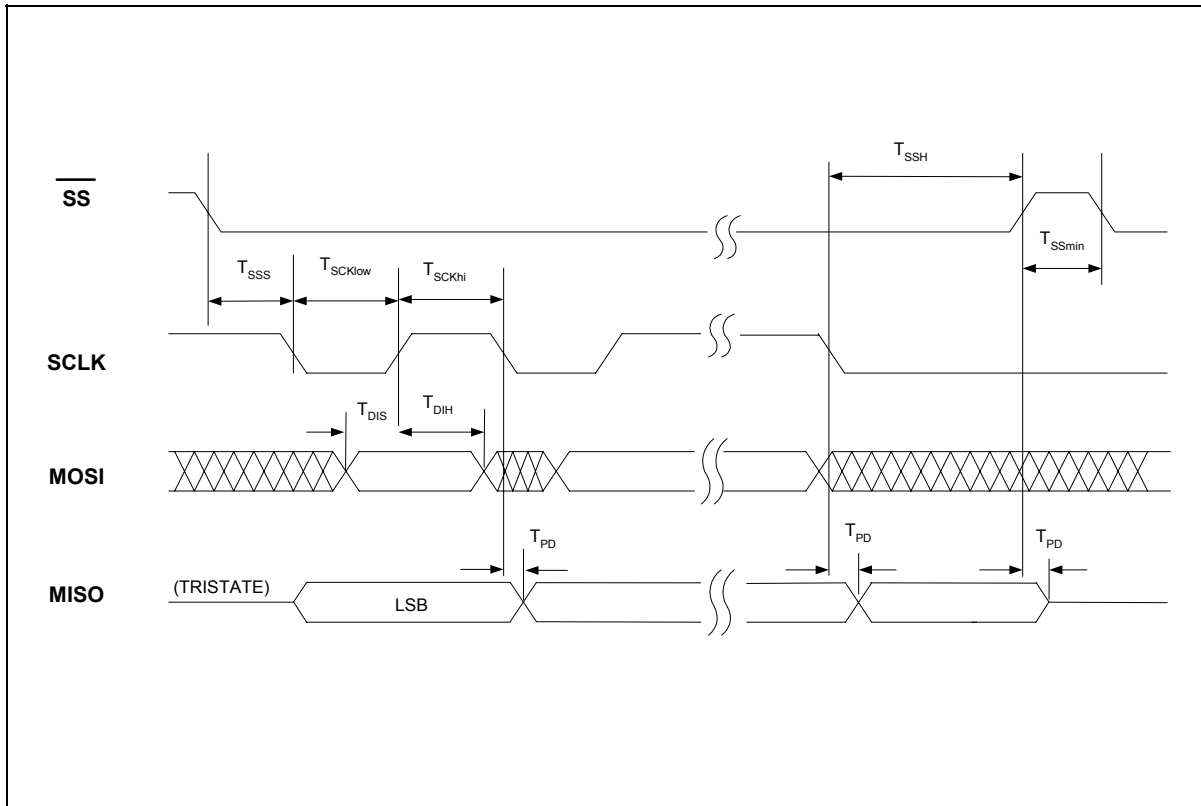


Figure 12.4: SPI Operation

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
SS Setup Time	T_{SSS}	500			nsec
SS Hold Time	T_{SSH}	500			nsec
Data in Setup Time	T_{DIS}	200			nsec
Data in Hold Time	T_{DIH}	200			nsec
Output Delay	T_{PD}			500	nsec
Output Delay to HighZ	T_{DF}			500	nsec
SS HIGH	T_{SSmin}	1			μ sec
SCLK High Time	T_{SCKhi}	400			nsec
SCLK Low Time	T_{SCKlow}	400			nsec
CLK Frequency	F_0			1,000	KHz
Power-Up Delay ^[1]	T_{PUD}		50		msec

Note: ^[1] All timing parameters are based upon 8 kHz sampling frequency.

ISD1700 SERIES



13 ABSOLUTE MAXIMUM RATINGS

ABSOLUTE MAXIMUM RATINGS (DIE) ^[1]

Condition	Value
Junction temperature	150°C
Storage temperature range	-65°C to +150°C
Voltage Applied to any pads	(V _{SS} - 0.3V) to (V _{CC} + 0.3V)
Power supply voltage to ground potential	-0.3V to +7.0V

ABSOLUTE MAXIMUM RATINGS (PACKAGED PARTS) ^[1]

Condition	Value
Junction temperature	150°C
Storage temperature range	-65°C to +150°C
Voltage Applied to any pins	(V _{SS} - 0.3V) to (V _{CC} + 0.3V)
Voltage applied to any pin (Input current limited to +/-20 mA)	(V _{SS} - 1.0V) to (V _{CC} + 1.0V)
Power supply voltage to ground potential	-0.3V to +7.0V

^[1] Stresses above those listed may cause permanent damage to the device. Exposure to the absolute maximum ratings may affect device reliability. Functional operation is not implied at these conditions.

ISD1700 SERIES



13.1 OPERATING CONDITIONS

OPERATING CONDITIONS (DIE)

CONDITIONS	VALUES
Operating temperature range	0°C to +50°C
Supply voltage (V_{CC}) ^[1]	+2.4 V to +5.5 V
Ground voltage (V_{SS}) ^[2]	0 V
Input voltage (V_{CC}) ^[1]	0 V to 5.5 V
Voltage applied to any pins	($V_{SS} - 0.3$ V) to ($V_{CC} + 0.3$ V)

OPERATING CONDITIONS (PACKAGED PARTS)

CONDITIONS	VALUES
Operating temperature range (Case temperature)	-40°C to +85°C
Supply voltage (V_{DD}) ^[1]	+2.4V to +5.5V
Ground voltage (V_{SS}) ^[2]	0V
Input voltage (V_{DD}) ^[1]	0V to 5.5V
Voltage applied to any pins	($V_{SS} - 0.3$ V) to ($V_{DD} + 0.3$ V)

^[1] $V_{CC} = V_{CCA} = V_{CCD} = V_{CCP}$

^[2] $V_{SS} = V_{SSA} = V_{SSD} = V_{SSP1} = V_{SSP2}$



ISD1700 SERIES

14 ELECTRICAL CHARACTERISTICS

14.1 DC PARAMETERS

PARAMETER	SYMBOL	MIN	TYP ^[1]	MAX	UNITS	CONDITIONS	
Supply Voltage	V_{DD}	2.4		5.5	V		
Input Low Voltage	V_{IL}	$V_{SS}-0.3$		$0.3 \times V_{DD}$	V		
Input High Voltage	V_{IH}	$0.7 \times V_{DD}$		V_{DD}	V		
Output Low Voltage	V_{OL}	$V_{SS}-0.3$		$0.3 \times V_{DD}$	V	$I_{OL} = 4.0 \text{ mA}$ ^[2]	
Output High Voltage	V_{OH}	$0.7 \times V_{DD}$		V_{DD}	V	$I_{OH} = -1.6 \text{ mA}$ ^[2]	
Record Current	I_{DD_Record}		20		mA	$V_{DD} = 5.5 \text{ V}$, No load, Sampling freq = 12 kHz	
Playback Current	$I_{DD_Playback}$		20		mA		
Erase Current	I_{DD_Erase}		20		mA		
Standby Current	I_{SB}		0.5	1	μA	$V_{DD} = 5.5 \text{ V}$, $T = 25^\circ\text{C}$ ^{[3] [4]}	
Input Leakage Current	I_{ILPD1}			± 1	μA	Force V_{DD}	
Input Current Low	I_{ILPD2}	-3		-10	μA	Force V_{SS} , others at V_{CC}	
Preamp Input Impedance	R_{MIC+}, R_{MIC-}		7		k Ω	Power-up AGC	
AnalIn Input Impedance	R_{AnalIn}		42		k Ω	Power-up	
MIC Differential Input	V_{IN1}		15	300	mV	Peak-to-Peak ^[5]	
AnalIn Input Voltage	V_{IN2}			1	V	Peak-to-Peak	
Gain from MIC to SP+/-	A_{MSP}	6		40	dB	$V_{IN} = 15 \sim 300 \text{ mV}$, AGC = $4.7 \mu\text{F}$, $V_{CC} = 2.4 \text{ V} \sim 5.5 \text{ V}$	
Speaker Output Load	R_{SPK}	8			Ω	Across both Speaker pins	
Speaker Output Power	P_{out}		670		mW	$V_{DD} = 5.5 \text{ V}$	1Vp-p, 1 kHz sine wave at AnalIn. R_{SPK} = 8 Ω .
			313		mW	$V_{DD} = 4.4 \text{ V}$	
			117		mW	$V_{DD} = 3 \text{ V}$	
			49		mW	$V_{DD} = 2.4 \text{ V}$	
Speaker Output Voltage	V_{OUT1}		V_{DD}		V	$R_{SPK} = 8 \Omega$ (Speaker), Typical buzzer	
AUD	I_{AUD}		-3.0		mA	$V_{DD} = 4.5 \text{ V}$, $R_{EXT} = 390 \Omega$	
Total Harmonic Distortion	THD		1		%	15 mV p-p 1 kHz sine wave, Cmessage weighted	

Notes: ^[1] Conditions: $V_{CC} = 4.5 \text{ V}$, 8 kHz sampling frequency and $T_A = 25^\circ\text{C}$, unless otherwise stated.

^[2] LED output during Record operation.

^[3] V_{CCA} , V_{CCD} and V_{CCP} are connected together. V_{SSA} , V_{SSP1} , V_{SSP2} and V_{SSD} are connected together.

^[4] **REC**, **PLAY**, **FT**, **FWD**, **ERASE**, **VOL** and **RESET** must be at V_{CCD} .

^[5] Balanced input signal applied between MIC+ and MIC- as shown in the applications example. Single-ended MIC+ or MIC- input is recommended to be less than 100 mV p-p.

ISD1700 SERIES



14.2 AC PARAMETERS

CHARACTERISTIC	SYMBOL	MIN	TYP ^[1]	MAX	UNITS	CONDITIONS	
Sampling Frequency ^[2]	F _S	4		12	kHz	V _{CC} =2.4 V~5.5V	
Duration ^[3]	T _{Dur}		Section 6.1.2		sec	V _{CC} =2.4 V~5.5V, all F _S	
Rising time	T _r	0		100	nsec		
Falling Time	T _f	0		100	nsec		
Debounce Time (REC, PLAY, ERASE, FWD, VOL)	T _{Deb}		16		msec	F _S =12 kHz	V _{CC} =2.4 V~5.5 V
			24		msec	F _S =8 kHz	
			30		msec	F _S =6.4 kHz	
			37		msec	F _S =5.3 kHz	
			48		msec	F _S =4 kHz	
RESET Pulse	T _{RESET}	1			μsec	V _{CC} =2.4 V~5.5 V	
Record SetUp Time	T _{RSetUp}		0.37		sec	F _S =12 kHz	V _{CC} =2.4 V~5.5 V, with SEs played
			0.54		sec	F _S =8 kHz	
			0.67		sec	F _S =6.4 kHz	
			0.80		sec	F _S =5.3 kHz	
			1.05		sec	F _S =4 kHz	
Record Stop Time	T _{RStop}		0.35		sec	F _S =12 kHz	V _{CC} =2.4 V~5.5 V, with SEs played
			0.52		sec	F _S =8 kHz	
			0.65		sec	F _S =6.4 kHz	
			0.77		sec	F _S =5.3 kHz	
			1.03		sec	F _S =4 kHz	
Play SetUp Time	T _{PSetUp}		100		msec	V _{CC} =2.4 V~5.5 V, all F _S	
Play Stop Time	T _{PStop}		33		msec	V _{CC} =2.4 V~5.5 V, all F _S	
Erase Stop Time	T _{EStop}		0.34		sec	F _S =12 kHz	V _{CC} =2.4 V~5.5 V, with SEs played
			0.51		sec	F _S =8 kHz	
			0.64		sec	F _S =6.4 kHz	
			0.77		sec	F _S =5.3 kHz	
			1.02		sec	F _S =4 kHz	
AUD Ramp Up Time	T _{RU}		4		msec	V _{CC} =2.4 V~5.5 V	
AUD Ramp down Time	T _{RD}		4		msec	V _{CC} =2.4 V~5.5 V	
LED Cycle frequency	T _{Cyc}	1		6	Hz	Playback at any F _S	

Notes: ^[1] Typical values: V_{CC} = 4.5 V, SF = 8 kHz and @ T_A = 25°C, unless otherwise stated.

^[2] Sampling Frequency can vary as much as ±2.25 percent over the temperature and voltage ranges.

^[3] Duration can vary as much as ±2.25 percent over the commercial temperature and voltage ranges.

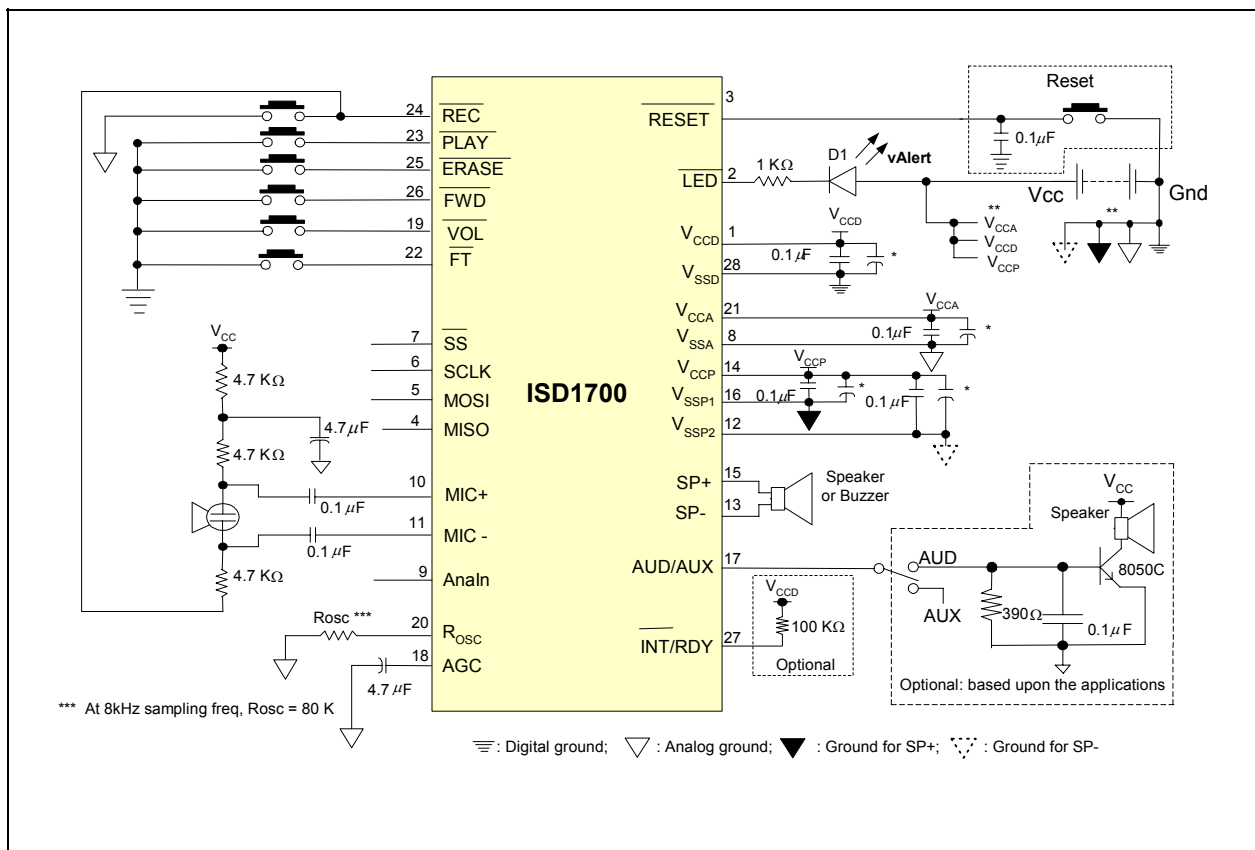
15 TYPICAL APPLICATION CIRCUITS

The following typical applications examples on ISD1700 Series are for references only. They make no representation or warranty that such applications shall be suitable for the use specified. Each design has to be optimized in its own system for the best performance on voice quality, current consumption, functionalities and etc.

The below notes apply to the following applications examples:

- * These capacitors may be needed in order to optimize for the best voice quality, which is also dependent upon the layout of the PCB. Depending on system requirements, they can be 10 μF , 4.7 μF or other values. Please refer to the applications notes or consult Winbond for layout advice.
- ** It is important to have a separate path for each ground and power back to the related terminals to minimize the noise. Also, the power supplies should be decoupled as close to the device as possible.

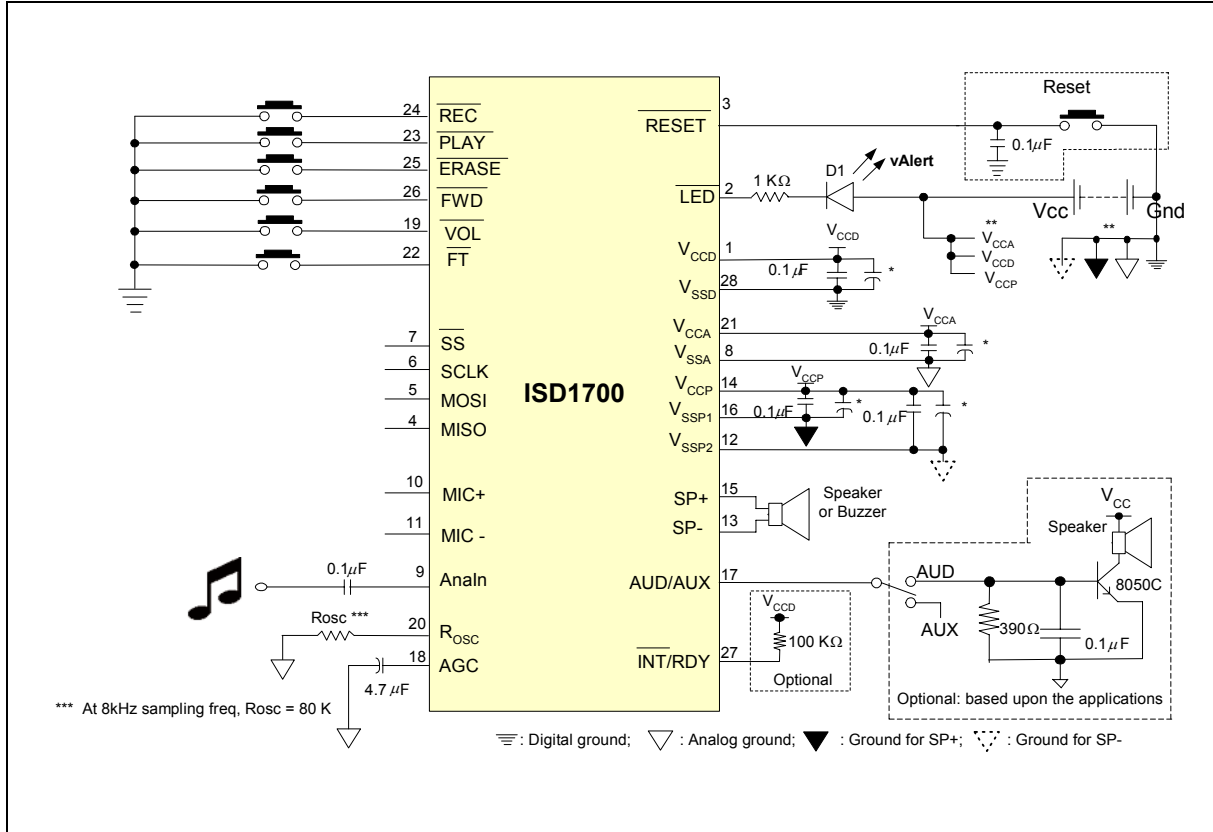
Example #1: Recording using microphone input via push-button controls



ISD1700 SERIES



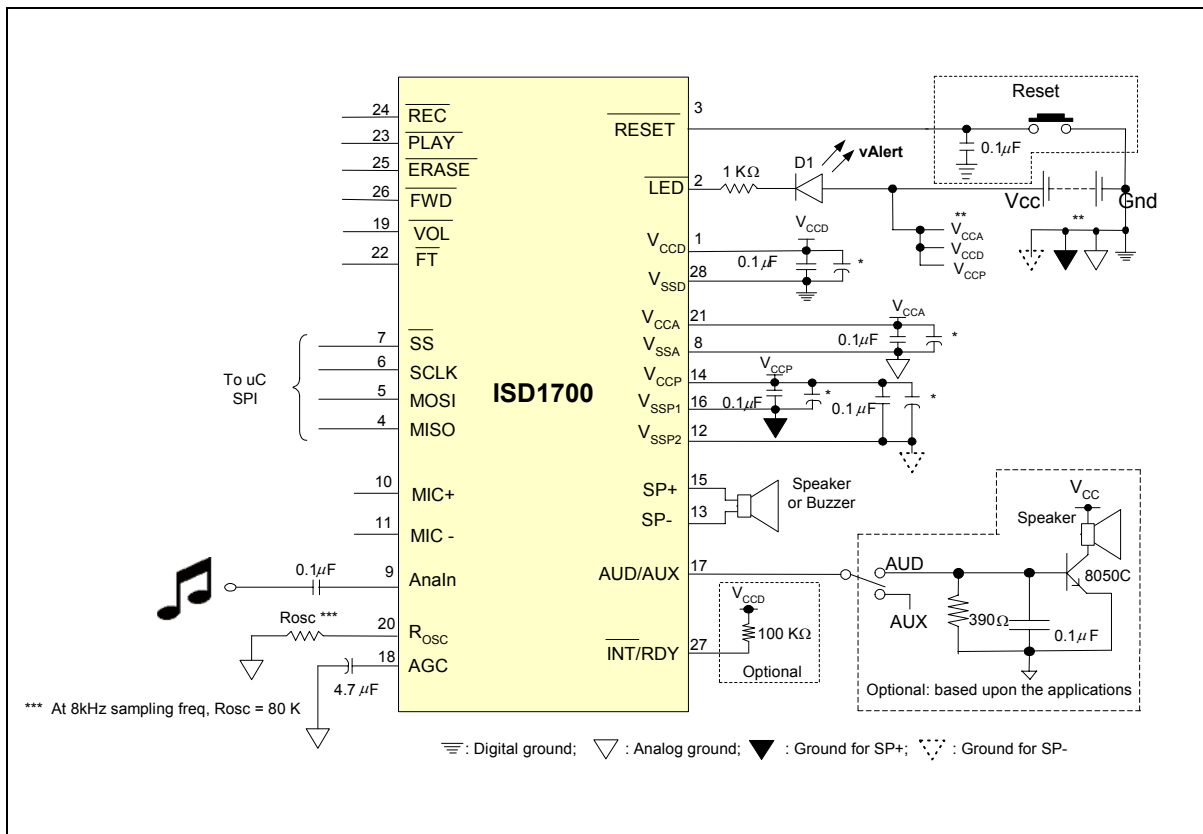
Example #2: Recording using Analn input via push-button controls



ISD1700 SERIES



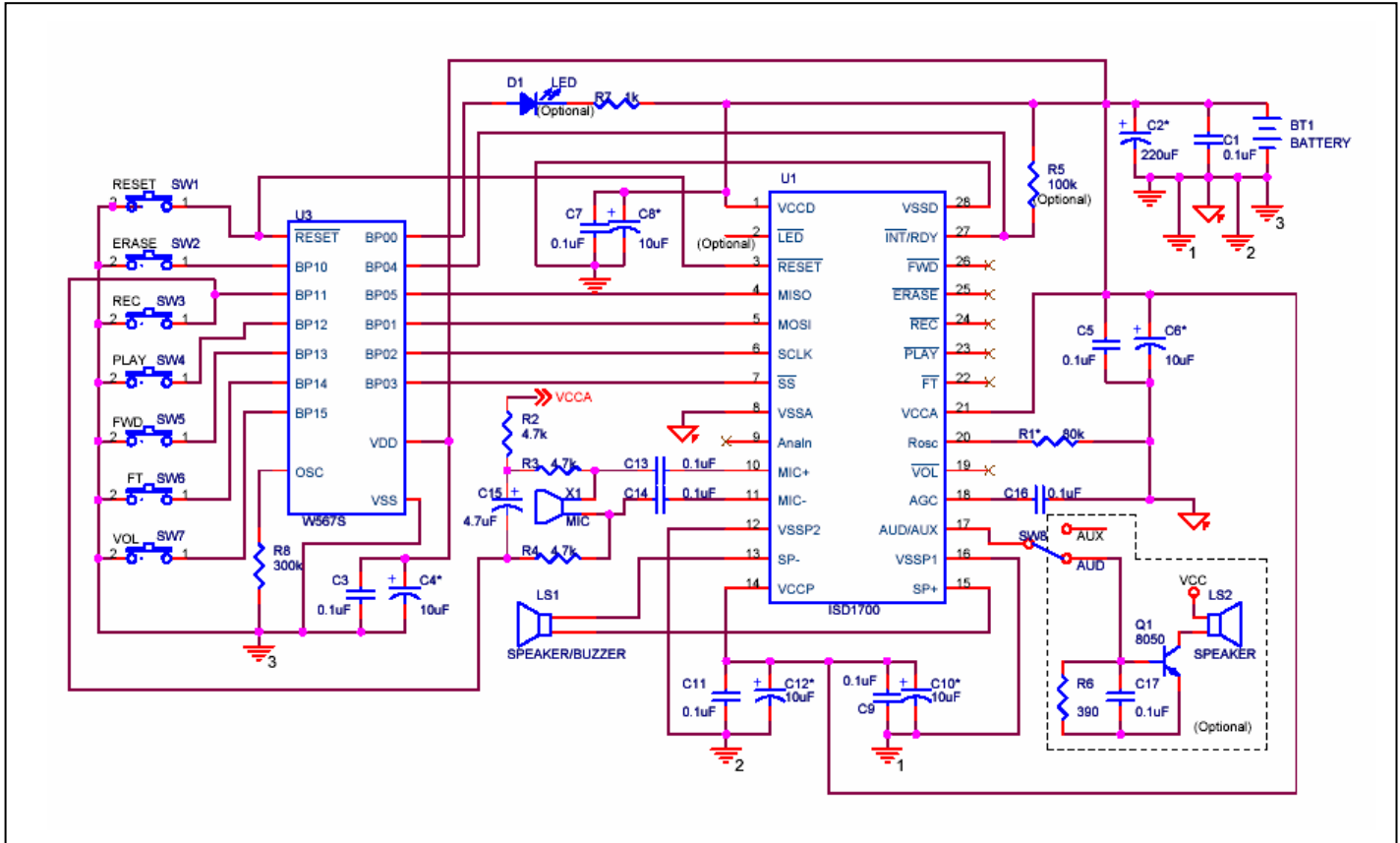
Example #3: Connecting the SPI Interface to a microcontroller



ISD1700 SERIES



Example #4: Connecting the ISD1700 with PowerSpeech W567



15.1 GOOD AUDIO DESIGN PRACTICES

To ensure the highest quality of voice reproduction, it is important to follow good audio design practices in layout and power supply decoupling. See recommendations from below links or other Application Notes in our websites.

Good Audio Design Practices

http://www.winbond-usa.com/products/isd_products/chipcorder/applicationinfo/apin11.pdf

Single-Chip Board Layout Diagrams

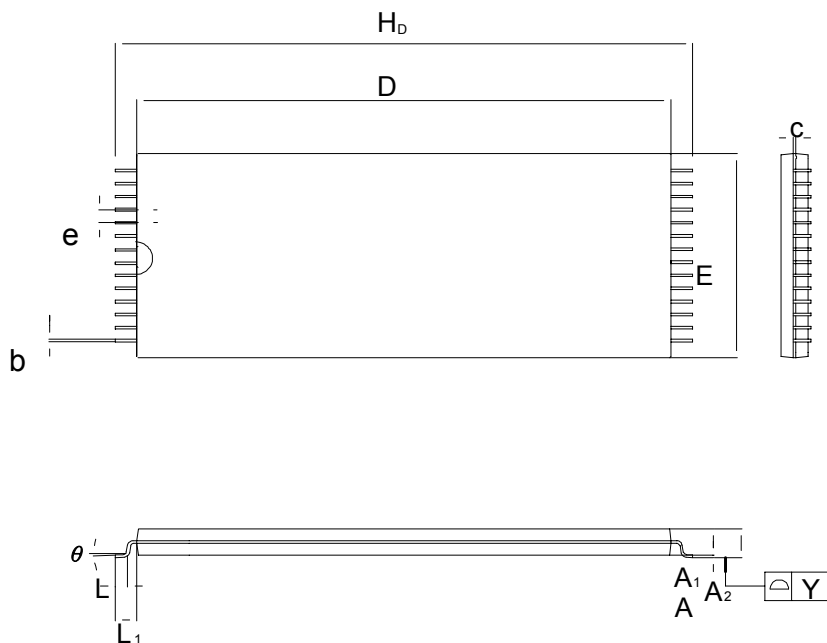
http://www.winbond-usa.com/products/isd_products/chipcorder/applicationinfo/apin12.pdf

ISD1700 SERIES



16 PACKAGING

16.1 28-LEAD 8X13.4MM PLASTIC THIN SMALL OUTLINE PACKAGE (TSOP) TYPE 1 - IQC

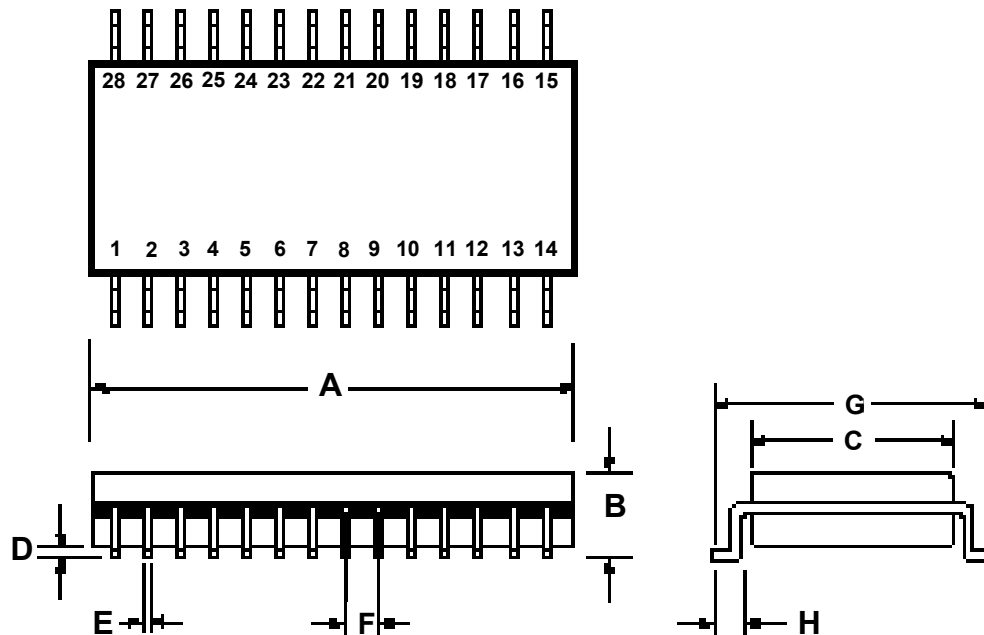


Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.047	—	—	1.20
A ₁	0.002	—	0.006	0.05	—	0.15
A ₂	0.035	0.040	0.041	0.95	1.00	1.05
b	0.007	0.008	0.011	0.17	0.20	0.27
c	0.004	0.006	0.008	0.10	0.15	0.21
D	0.461	0.465	0.469	11.70	11.80	11.90
E	0.311	0.315	0.319	7.90	8.00	8.10
H _b	0.520	0.528	0.536	13.20	13.40	13.60
e	—	0.022	—	—	0.55	—
L	0.020	0.024	0.028	0.50	0.60	0.70
L ₁	—	0.031	—	—	0.80	—
Y	0.000	—	0.004	0.00	—	0.10
θ	0	3	5	0	3	5

ISD1700 SERIES



16.2 28-LEAD 300-MIL PLASTIC SMALL OUTLINE INTEGRATED CIRCUIT (SOIC)



Plastic Small Outline Integrated Circuit (SOIC) Dimensions

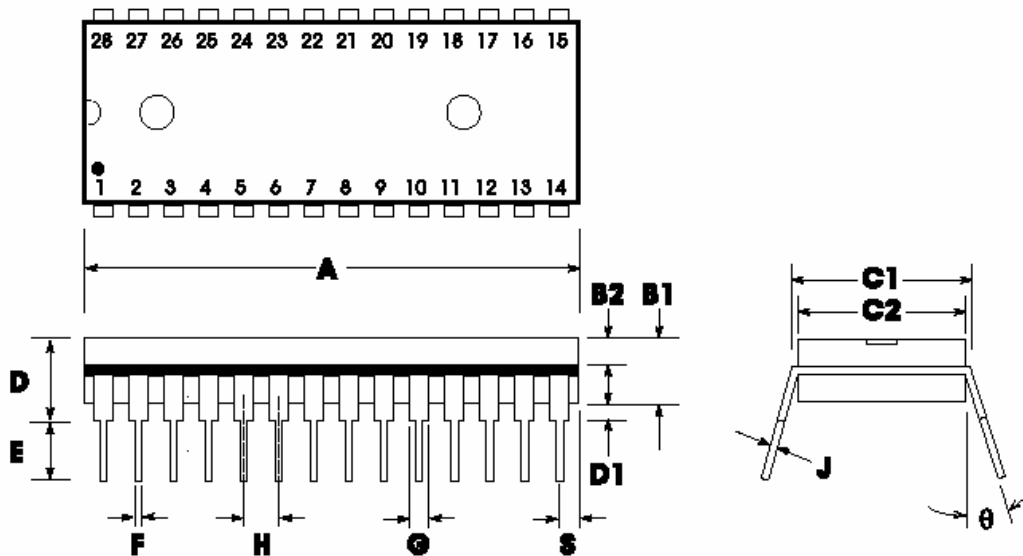
	INCHES			MILLIMETERS		
	Min	Nom	Max	Min	Nom	Max
A	0.701	0.706	0.711	17.81	17.93	18.06
B	0.097	0.101	0.104	2.46	2.56	2.64
C	0.292	0.296	0.299	7.42	7.52	7.59
D	0.005	0.009	0.0115	0.127	0.22	0.29
E	0.014	0.016	0.019	0.35	0.41	0.48
F		0.050			1.27	
G	0.400	0.406	0.410	10.16	10.31	10.41
H	0.024	0.032	0.040	0.61	0.81	1.02

Note: Lead coplanarity to be within 0.004 inches.

ISD1700 SERIES



16.3 28-LEAD 600-MIL PLASTIC DUAL INLINE PACKAGE (PDIP)



Plastic Dual In-Line Package (PDIP) (P) Dimensions

	INCHES			MILLIMETERS		
	Min	Nom	Max	Min	Nom	Max
A	1.445	1.450	1.455	36.70	36.83	36.96
B1		0.150			3.81	
B2	0.065	0.070	0.075	1.65	1.78	1.91
C1	0.600		0.625	15.24		15.88
C2	0.530	0.540	0.550	13.46	13.72	13.97
D			0.19			4.83
D1	0.015			0.38		
E	0.125		0.135	3.18		3.43
F	0.015	0.018	0.022	0.38	0.46	0.56
G	0.055	0.060	0.065	1.40	1.52	1.65
H		0.100			2.54	
J	0.008	0.010	0.012	0.20	0.25	0.30
S	0.070	0.075	0.080	1.78	1.91	2.03
theta	0°		15°	0°		15°

16.4 DIE INFORMATION

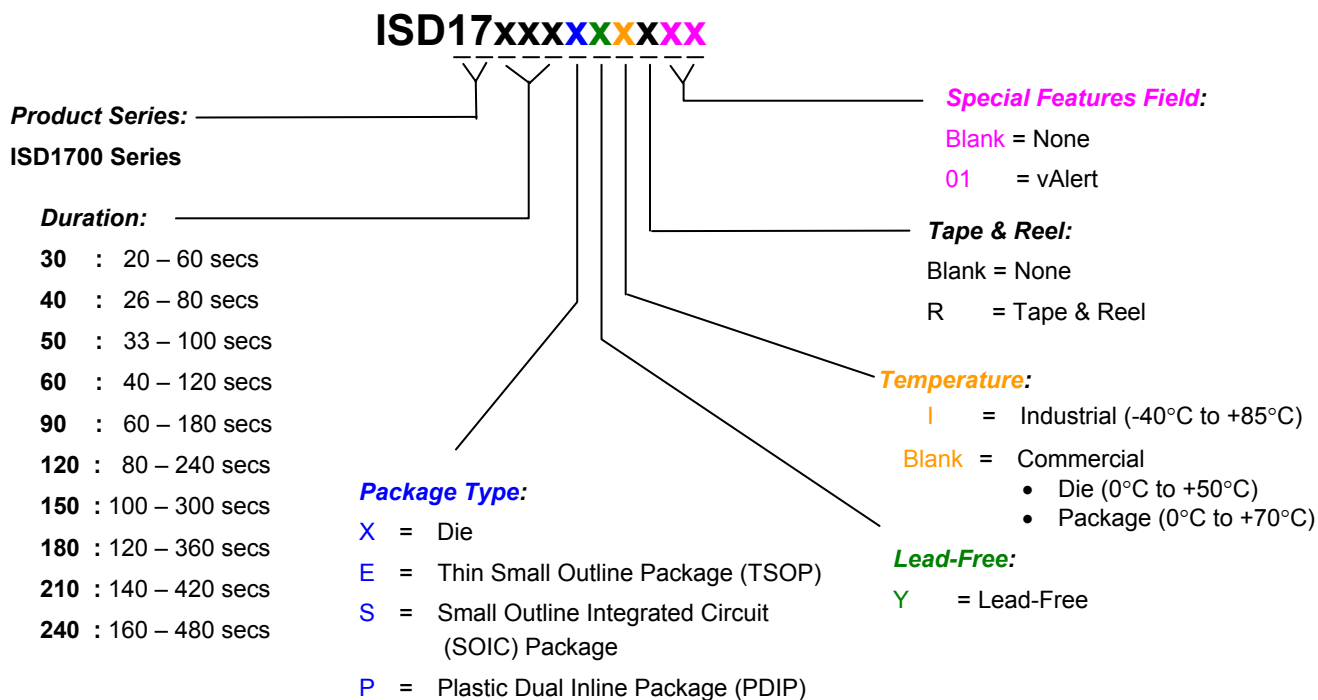
For die info, please contact the local Winbond Sales Representatives.



ISD1700 SERIES

17 ORDERING INFORMATION

Product Number Descriptor Key



When ordering ISD1700 devices, please refer to the above ordering scheme. Contact the local Winbond Sales Representatives for any questions and availability information.

For the latest product information, please access Winbond's worldwide web site at <http://www.winbond-usa.com>

ISD1700 SERIES**18 VERSION HISTORY**

VERSION	DATE	DESCRIPTION
0	July 2005	Initial version
0.1	Aug 2005	Revise INT to /INT Revise MISO pin description Add Switching from SPI mode to User mode section Update SPI command reference table Add operating conditions for packaged units Add application examples Update TSOP package info
1.0	Sep 2005	Revise APC register Revise operating condition section Update application examples
1.1	Dec 2005	Revise max. row address Revise operating paths in APC register Revise standalone operation overview Add Restoring Circular memory architecture section Add EXTCLK feature
1.2	Jan 2006	Update Pb-free info and remove leaded option Revise memory array architecture Update circular memory array architecture sections Revise description of global erase in standalone mode Update SPI mode section and SPI command reference section Revise timing diagram for record Update application circuits section

ISD1700 SERIES



Winbond products are not designed, intended, authorized or warranted for use as components in systems or equipment intended for surgical implantation, atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, or for other applications intended to support or sustain life. Furthermore, Winbond products are not intended for applications wherein failure of Winbond products could result or lead to a situation wherein personal injury, death or severe property or environmental damage could occur.

Winbond customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Winbond for any damages resulting from such improper use or sales.

The contents of this document are provided only as a guide for the applications of Winbond products. Winbond makes no representation or warranties with respect to the accuracy or completeness of the contents of this publication and reserves the right to discontinue or make changes to specifications and product descriptions at any time without notice. No license, whether express or implied, to any intellectual property or other right of Winbond or others is granted by this publication. Except as set forth in Winbond's Standard Terms and Conditions of Sale, Winbond assumes no liability whatsoever and disclaims any express or implied warranty of merchantability, fitness for a particular purpose or infringement of any Intellectual property.

The contents of this document are provided "AS IS", and Winbond assumes no liability whatsoever and disclaims any express or implied warranty of merchantability, fitness for a particular purpose or infringement of any Intellectual property. In no event, shall Winbond be liable for any damages whatsoever (including, without limitation, damages for loss of profits, business interruption, loss of information) arising out of the use of or inability to use the contents of this documents, even if Winbond has been advised of the possibility of such damages.

Application examples and alternative uses of any integrated circuit contained in this publication are for illustration only and Winbond makes no representation or warranty that such applications shall be suitable for the use specified.

The 100-year retention and 100K record cycle projections are based upon accelerated reliability tests, as published in the Winbond Reliability Report, and are neither warranted nor guaranteed by Winbond. This product incorporates SuperFlash®.

This datasheet and any future addendum to this datasheet is(are) the complete and controlling ISD® ChipCorder® product specifications. In the event any inconsistencies exist between the information in this and other product documentation, or in the event that other product documentation contains information in addition to the information in this, the information contained herein supersedes and governs such other information in its entirety. This datasheet is subject to change without notice.

Copyright© 2005, Winbond Electronics Corporation. All rights reserved. ChipCorder® and ISD® are trademarks of Winbond Electronics Corporation. SuperFlash® is the trademark of Silicon Storage Technology, Inc. All other trademarks are properties of their respective owners.

**Headquarters**

No. 4, Creation Rd. III
Science-Based Industrial Park,
Hsinchu, Taiwan
TEL: 886-3-5770066
FAX: 886-3-5665577
<http://www.winbond.com.tw/>

Winbond Electronics Corporation America

2727 North First Street, San Jose,
CA 95134, U.S.A.
TEL: 1-408-9436666
FAX: 1-408-5441797
<http://www.winbond-usa.com/>

Winbond Electronics (Shanghai) Ltd.

27F, 299 Yan An W. Rd. Shanghai,
200336 China
TEL: 86-21-62365999
FAX: 86-21-62356998

Taipei Office

9F, No. 480, Pueiguang Rd.
Neihu District
Taipei, 114 Taiwan
TEL: 886-2-81777168
FAX: 886-2-87153579

Winbond Electronics Corporation Japan

7F Daini-ueno BLDG. 3-7-18
Shinyokohama Kohokuku,
Yokohama, 222-0033
TEL: 81-45-4781881
FAX: 81-45-4781800

Winbond Electronics (H.K.) Ltd.

Unit 9-15, 22F, Millennium City,
No. 378 Kwun Tong Rd.,
Kowloon, Hong Kong
TEL: 852-27513100
FAX: 852-27552064

Please note that all data and specifications are subject to change without notice.
All the trademarks of products and companies mentioned in this datasheet belong to their respective owners.